Product Technical Specification

Fastrack Supreme IESM

Reference: **WA_DEV_Fastrk_PTS_001**

Revision: **002**

Date: **March 27, 2008**

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IESM

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Document History

Revision	Date	List of revisions	
001	September 19, 2007	Creation	
002	March 27, 2008	Updates	

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Overview

This document describes the electrical and mechanical features of the Internal Expansion Module, also known as IESM.

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Web Site Support

General information about Wavecom and its range of products:	www.wavecom.com
Specific support is available for the Fastrack Supreme Plug & Play Wireless CPU®:	www.wavecom.com/fastracksupreme
Carrier/Operator approvals:	www.wavecom.com/approvals
Open AT® Introduction:	www.wavecom.com/OpenAT
Developer support for software and hardware:	www.wavecom.com/forum

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1 References

1.1 Reference Documents

For more details, several reference documents can be consulted. The Wavecom reference documents are provided in the Wavecom documents package contrary at the general reference documents, which are not Wavecom owned.

1.1.1 Fastrack Supreme 10/20 and IESM Documents

[1] Fastrack Supreme User Guide (Ref: WA_DEV_Fastrk_UGD_001)

[2] IESM-GPS+USB User Guide (Ref: WA_DEV_Fastrk_UGD_002)

[3] ESM-GPS+USB Installation Guide (Ref: WA_DEV_Fastrk_UGD_003)

[4] IESM-IO+USB User Guide (Ref: WA_DEV_Fastrk_UGD_006)

[5] IESM-IO+USB Installation Guide (Ref: WA_DEV_Fastrk_UGD_005)

[6] IESM-IO+USB+GPS User Guide (Ref: WA_DEV_Fastrk_UGD_008)

[7] IESM-IO+USB+GPS Installation Guide (Ref: WA_DEV_Fastrk_UGD_007)

1.1.2 Open AT® Software Documents

[8] Getting started with Open AT® SDK v4.22 (Ref:WM_DEV_OAT_UGD_048)

[9] Tutorial for Open AT® IDE v1.04 (Ref:WM_DEV_OAT_UGD_044)

[10] Tools Manual for Open AT® IDE v1.04 (Ref:WM_DEV_OAT_UGD_045)

[11] Basic Development Guide for Open AT® v4.21 (Ref:WM_DEV_OAT_UGD_050)

[12] ADL User Guide for Open AT® v4.21 (Ref:WM_DEV_OAT_UGD_051)

[13] Open AT® v4.22 Official Release Note (Ref:WM_DEV_OAT_DVD_338)

1.1.3 AT Software Documents

[14] AT commands interface Guide for FW v6.63 (Ref:WM_DEV_OAT_UGD_049)

[15] Open AT® Firmware v6.63 Customer Release Note (Ref:WM_PGM_OAT_CRN_001)

1.1.4 Open AT Plug-In Documents

[16] C-GPS Overview and Usage (Ref:WM_DEV_C-GPS_APN_001)

[17] C-GPS Development Kit User Guide (Ref:WM_DEV_C-GPS_UGD_001)

[18] eRide Datasheet for Prelude and Opus 1 (Ref:WM_DEV_C-GPS_UGD_002)

[19] eRide C-GPS Core Interface Rev 1.16.02 (Ref:WM_DEV_C-GPS_IFS_003)

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1.1.5 General Reference Documents

[20] "I²C Bus Specification", Version 2.0, Philips Semiconductor 1998

[21] ISO 7816-3 Standard

1.2 Abbreviations

Abbreviation	Definition
AC	Alternative Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analogue Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EDGE	Enhance Data rates for GSM Evolution
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EGPRS	Enhance GPRS

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Abbreviation	Definition
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)

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Abbreviation	Definition
PBCCH	Packet Broadcast Control CHannel
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Wireless CPU®
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

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Abbreviation	Definition
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio

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2 General Description

2.1 General Information

IESM is an add-on board for Fastrack Supreme 10/20 to expand its functionality into complete customizable application. By utilizing the available Internal Expansion Socket (IES) on the standard Fastrack Supreme 10/20, this can be turned into various machine to machine applications by simply plugging-in.

Fastrack Supreme with IESM plugged-in may utilize one or more Open AT® Plug-Ins of the powerful open AT® software suite. Open AT® is the world's most comprehensive cellular development environment, which allows embedded standard ANSI C applications to be natively executed directly on the Wireless CPU®.

2.1.1 IESM Features

The lists of interfaces available on the 50-pin IES connector are as follows:

- 1 - UART Interface
- 6 – GPIOs
- 2 - SPI Bus
- 1- DAC
- 1- ADC
- 1 - USB
- 1 – PCM
- 1 – DTR
- 1 – Interrupt Pin
- RESET access to Wireless CPU®
- Interrupt Pin of Wireless CPU®
- Boot Pin of Wireless CPU®
- 2.8V Digital Power Supply from Wireless CPU®
- 1.8V Digital Power Supply from Wireless CPU®
- 2.8V Power Supply from Supreme board LDO
- 4V Power Supply from Supreme board
- 5.5V~32V External DC input

2.1.2 Operating System

- The release will be OASIS 0.1.3 with:
  - Firmware 6.63
  - OS 4.21
  - IDE 1.04

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2.1.3 Connection Interfaces

IESM board is possible to have three external connections:

- MMCX Connector
- Mini-B USB Connector
- 16 – Way IO Expander Socket

2.1.4 Environment and Mechanics

- Green policy: RoHS compliant

In order for the Fastrack Supreme 10/20 to be fully ROHS compliant, the add-on board IESM must also comply on this directive.

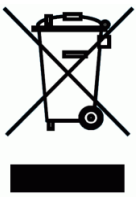
RoHS Directive

The Fastrack Supreme is now compliant with RoHS Directive 2002/95/EC, which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)".

Plug & Plays which are compliant with this directive are identified by the RoHS logo on their label.

Disposing of the product

This electronic product is subject to the EU Directive 2002/96/EC for Waste Electrical and Electronic Equipment (WEEE). As such, this product must not be disposed off at a municipal waste collection point. Please refer to local regulations for directions on how to dispose off this product in an environmental friendly manner.



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2.2 IES Functional Description

The global architecture of IESM is described below:

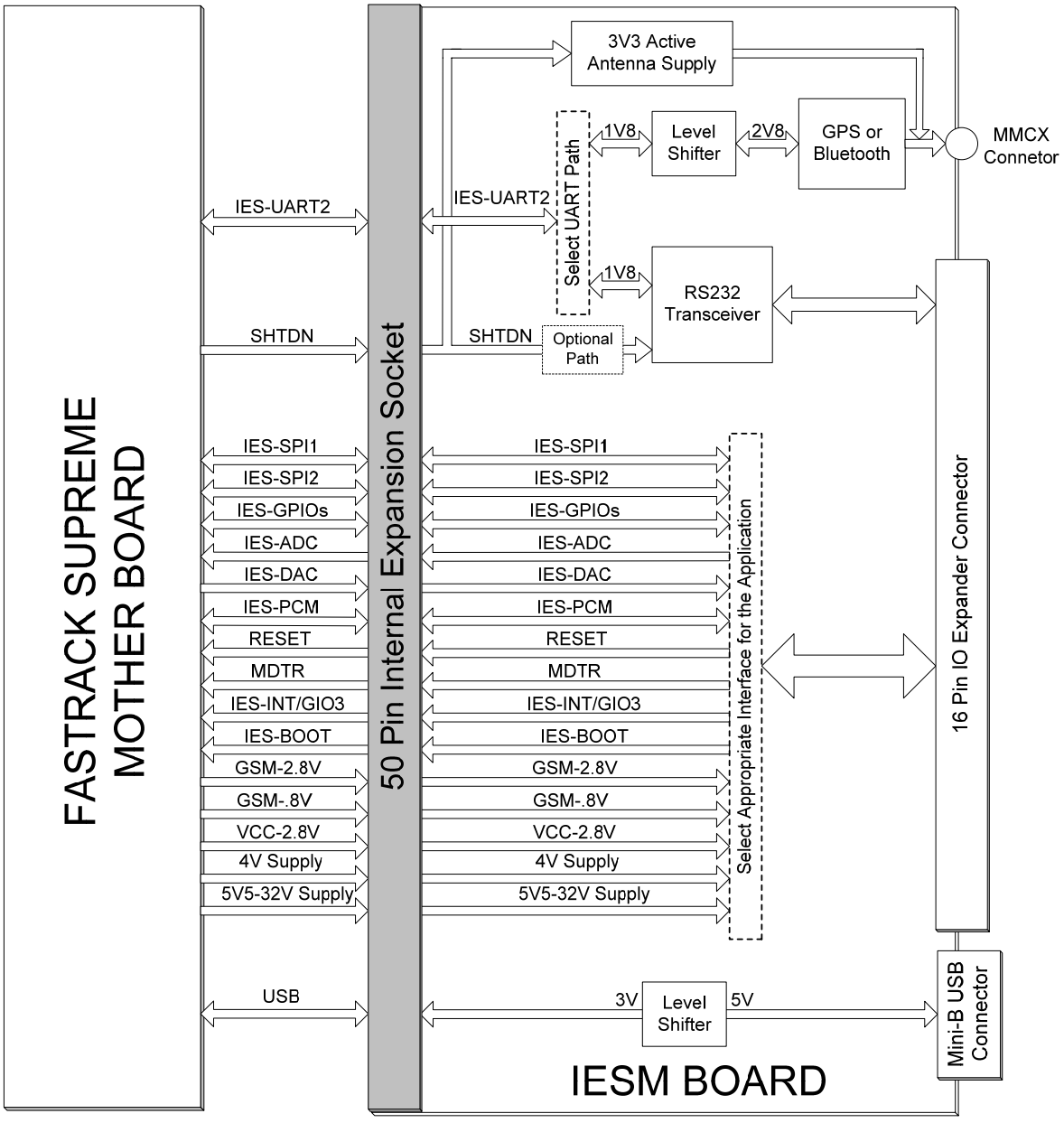

Figure 1: Functional architecture

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2.3 Operating System

The IESM is designed to integrate with the Fastrack Supreme 10/20 which is Open AT® compliant. With Open AT® and IESM, specific process applications could be performed for various types of vertical applications such as telemetry, multimedia, etc.

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3 Interfaces

3.1 General Purpose Connector (GPC)

A 50-pin connector is provided on the Fastrack Supreme 10/20 to interface with IESM containing either serial interface, USB, GPS, Bluetooth, LCD module or other application.

The interfaces available on the GPC are described below:

Chapter	Name	Driven by AT commands	Driven by Open AT®
3.4	Serial Interface		X
3.5	Auxiliary UART2 Serial Link	X	X
3.6	General Purpose IO	X	X
3.7	Analog to Digital Converter	X	X
3.8	Digital to Analog Converter		X
3.11	External Interrupt	X	X
3.13	Digital Audio Interface (PCM)	X	X
3.14	USB 2.0 Interface	X	X

3.2 Power Supply

3.2.1 Power Supply Output Description

The IESM power supplies are already available on the 50-pin connector.

Table describes the available supplies on the Internal Expansion Socket (IES).

Pin description

Signal	Pin number	I/O type	Description
VCC-2V8	41	Supply	LDO
4V	46, 47	Supply	High current power supply
DC-IN IESM	43, 44	Supply	High current external power supply. The same supply provided on the 4 Pin Micro-Fit connector with polarity protection

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Electrical characteristics of each DC supply signal

Parameter		Min	Typ	Max	Unit
VCC-2V8	Output voltage	2.73	2.8	2.87	V
	Output Current	-	-	100	mA

Parameter		Min	Typ	Max	Unit
4V	Output voltage	3.91	4	4.12	V
	Output Current	-	-	300	mA

Parameter		Min	Typ	Max	Unit
DC-IN IESM	Output voltage	5.5	13.2	32	V
	Output Current	218	91	37.5	mA

Important :

The total maximum power dissipation of these three supplies must not exceed 1.2 W.

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3.3 Electrical Information for Digital I/O

The three types of digital I/O available are:

- 2.8 volt CMOS
- 1.8 volt CMOS
- Open drain

Electrical characteristics of digital I/O

2.8 volt type (2V8)						
Parameter		I/O type	Minim.	Typ	Maxim.	Condition
Internal 2.8V power supply		VCC_2V8	2.74V	2.8V	2.86V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.84V	
	V_{IH}	CMOS	1.96V		3.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	2.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

*Absolute maximum ratings

All 2.8V I/O pins do not accept input signal voltage above the maximum voltage specified in the above table.

1.8 volt type (1V8)						
Parameter		I/O type	Minim.	Typ	Maxim.	Condition
Internal 1V8 power supply		VCC_1V8	1.76V	1.8V	1.94V	
Input / Output pin	V_{IL}	CMOS	-0.5V*		0.54V	
	V_{IH}	CMOS	1.33V		2.2V*	
	V_{OL}	CMOS			0.4V	I_{OL} = - 4 mA
	V_{OH}	CMOS	1.4V			I_{OH} = 4 mA
	I_{OH}				4mA	
	I_{OL}				- 4mA	

*Absolute maximum ratings

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Open drain output type						
Signal name	Parameter	I/O type	Minimum	Typ	Maximum	Condition
SDA / GPIO27 and SCL / GPIO26	V_{TOL}	Open Drain			3.3V	Tolerated voltage
	V_{IH}	Open Drain	2V			
	V_{IL}	Open Drain			0.8V	
	V_{OL}	Open Drain			0.4V	
	I_{OL}	Open Drain			3mA	

The reset states of I/Os are given in each interface description chapter. Definitions of these states are given below:

Reset state definition	
Parameter	Definition
0	Set to GND
1	Set to supply 1V8 or 2V8 depending on I/O type
Pull-down	Internal pull-down with ~60K resistor.
Pull-up	Internal pull-up with ~60K resistor to supply 1V8 or 2V8 depending on I/O type.
Z	High impedance
Undefined	Caution: Undefined must not be used in your application if a special state is required at reset. These pins may be a toggling signal during reset.

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3.4 Serial Interface

The Fastrack Supreme IES may be connected to an LCD driver through either of the two SPI bus interface.

3.4.1 SPI Bus

Both SPI bus interfaces include:

- A CLK signal
- An I/O signal
- An I signal
- A CS signal complying with the standard SPI bus.

SPI bus characteristics:

- Master mode operation
- SPI speed is from 101.5 Kbit/s to 13 Mbit/s in master mode operation
- 3 or 4-wire interface
- SPI-mode configuration: 0 to 3
- 1 to 16 bits data length

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3.4.1.1 SPI Waveforms

Waveform for SPI transfer with 4-wire configuration in master mode 0 (chip select is not represented).

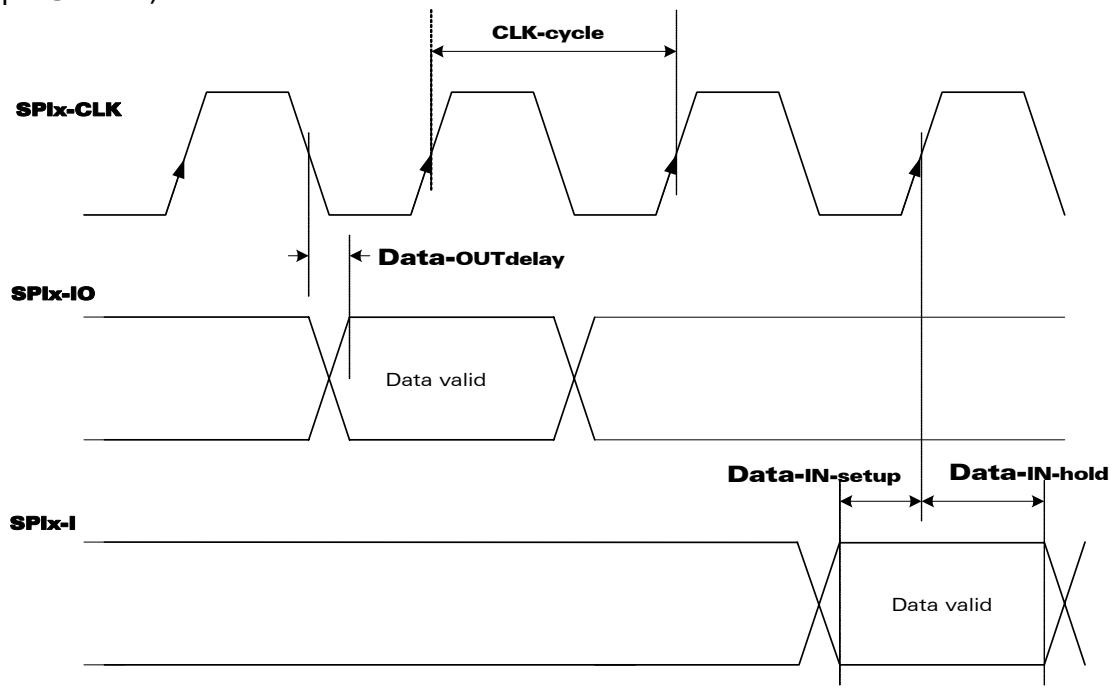

Figure 2: SPI Timing diagrams, Mode 0, Master, 4 wires

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
CLK-cycle	SPI clock frequency	0.1015		13	MHz
Data-OUT delay	Data-OUT ready delay time			10	ns
Data-IN-setup	Data-IN setup time	2			ns
Data-OUT-hold	Data-OUT hold time	2			ns

3.4.1.2 SPI Configuration

Operation	Maximum Speed	SPI-Mode	Duplex	3-wire type	4-wire type
Master	13 Mb/s	0,1,2,3	Half	SPIx-CLK; SPIx-IO; ~SPIx-CS	SPIx-CLK; SPIx-IO; SPIx-I; ~SPIx-CS

For the 4-wire configuration, SPIx-I/O is used as output only, SPIx-I is used as input only.

For the 3-wire configuration, SPIx-I/O is used as input and output.

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3.4.1.3 SPI1 Bus

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI1-CLK	16	O	2V8	Z	SPI Serial Clock	GPIO28
SPI1-IO	18	I/O	2V8	Z	SPI Serial input/output	GPIO29
SPI1-I	17	I	2V8	Z	SPI Serial input	GPIO30
~SPI1-CS	15	O	2V8	Z	SPI Enable	GPIO31

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.4.1.4 SPI2 Bus

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SPI2-CLK	19	O	2V8	Z	SPI Serial Clock	GPIO32
SPI2-IO	20	I/O	2V8	Z	SPI Serial input/output	GPIO33
SP2-I	22	I	2V8	Z	SPI Serial input	GPIO34
~SPI2-CS	21	O	2V8	Z	SPI Enable	GPIO35

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

3.4.2 I²C Bus

The I²C interface includes clock signal (SCL) and data signal (SDA) which complies with a 100Kbit/s-standard interface (standard mode: s-mode).

The I²C bus is always master.

The maximum speed transfer range is 400Kbit/s (fast mode: f-mode).

For more information on the bus, see the "I²C Bus Specification Version 2.0" [20] from PHILIPS.

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3.4.2.1 I²C Waveforms

I²C bus waveform in master mode configuration:

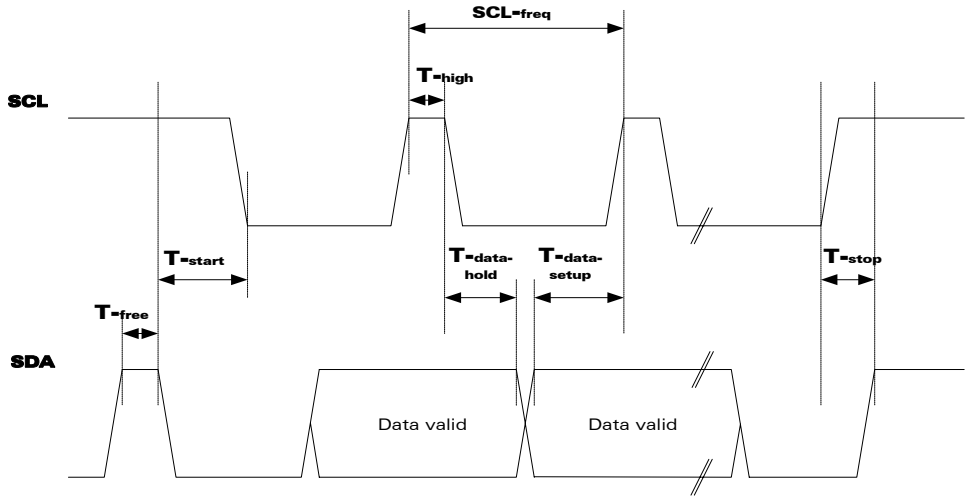

Figure 3: I²C Timing diagrams, Master

AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
SCL-freq	I²C clock frequency	100		400	KHz
T-start	Hold time START condition	0.6			µs
T-stop	Setup time STOP condition	0.6			µs
T-free	Bus free time, STOP to START	1.3			µs
T-high	High period for clock	0.6			µs
T-data-hold	Data hold time	0		0.9	µs
T-data-setup	Data setup time	100			ns

3.4.2.2 I²C Bus Pin-out

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
SCL	28	O	Open drain	Z	Serial Clock	GPIO26
SDA	30	I/O	Open drain	Z	Serial Data	GPIO27

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

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3.5 Auxiliary Serial Link (UART2)

The GPS or Bluetooth applications can be interface on auxiliary serial interface (UART2).

Pin description of UART2 interface

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
CT103 / TXD2*	24	I	1V8	Z	Transmit serial data	GPIO14
CT104 / RXD2*	23	O	1V8	Z	Receive serial data	GPIO15
~CT106 / CTS2*	25	O	1V8	Z	Clear To Send	GPIO16
~CT105 / RTS2*	26	I	1V8	Z	Request To Send	GPIO17

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

* According to PC view

Fastrack Supreme 10/20 are designed to operate using all the serial interface signals. In particular, it is mandatory to use RTS and CTS for hardware flow control in order to avoid data corruption during transmission.

The maximum baud rate of UART2 is **920**Kbit/s

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3.6 General Purpose Input/Output

The IES provides in total of 20 General Purpose I/O and available only if the multiplexed counterpart is not used. These can be used to control any external devices such as GPS, Bluetooth, LCD or other customer external applications.

Pin description of GPIO

Signal	Pin number	I/O	I/O type*	Reset state	Multiplexed with
GPIO3	32	I/O	1V8	Z	INT0
GPIO14	24	I/O	1V8	Z	CT103 / TXD2
GPIO15	23	I/O	1V8	Z	CT104 / RXD2
GPIO16	25	I/O	1V8	Z	~CT106 / CTS2
GPIO17	26	I/O	1V8	Z	~CT105 / RTS2
GPIO19	29	I/O	2V8	Z	Not mux
GPIO20	31	I/O	2V8	Undefined	Not mux
GPIO22	34	I/O	2V8	Z	Not mux*
GPIO23	33	I/O	2V8	Z	Not mux*
GPIO26	28	I/O	Open Drain	Z	SCL
GPIO27	30	I/O	Open Drain	Z	SDA
GPIO28	16	I/O	2V8	Z	SPI1-CLK
GPIO29	18	I/O	2V8	Z	SPI1-IO
GPIO30	17	I/O	2V8	Z	SP1-I
GPIO31	15	I/O	2V8	Z	~SPI1-CS
GPIO32	19	I/O	2V8	Z	SPI2-CLK
GPIO33	20	I/O	2V8	Z	SPI2-IO
GPIO34	22	I/O	2V8	Z	SP2-I
GPIO35	21	I/O	2V8	Z	~SPI2-CS
GPIO41	35	I/O	2V8	Z	~CT108-2 / DTR1

See chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and for Reset state definition.

* If a Bluetooth module is used, these GPIOs must be reserved.

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3.7 Analog to Digital Converter

One Analog to Digital Converter input is available at the IES connector. The converters are 10-bit resolution, ranging from 0 to 2V.

Pin description of the ADC

Signal	Pin number	I/O	I/O type	Description
AUX-ADC	14	I	Analog	A/D converter

Electrical characteristics of the ADC

Parameter		Min	Typ	Max	Unit
Resolution			10		bits
Sampling rate				138[1]	sps
Input signal range		0		2	V
INL (Integral non linearity)			15		mV
DNL (Differential non linearity)			2.5		mV
Input impedance	AUX-ADC		1M		Ω

* Internal pull-up to 2.8V

[1] Sampling rate only for AUX-ADC and Open AT® application

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3.8 Digital to Analogue Converter

One **D**igital to **A**nalog **C**onverter input is available at the IES connector. The converter is 8-bit resolution, ranging from 0 to 2.3V.

Pin description of the DAC

Signal	Pin number	I/O	I/O type	Description
AUX-DAC	40	O	Analog	D/A converter

This output assumes a typical external load of 2kΩ and 50pF in parallel.

Electrical characteristics of the DAC

Parameter	Min	Typ	Max	Unit
Resolution		8		bits
Output signal range	0		2.3	V
Output voltage after reset		1.147		V
INL (Integral non linearity)	-5		+5	LSB
DNL (Differential non linearity)	-1		+1	LSB

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3.9 BOOT Signal

A specific BOOT control pin is for downloading firmware for the Fastrack Supreme 10/20.

A specific PC software program, provided by Wavecom, is needed to perform this specific download.

The BOOT pin must be connected to VCC_1V8 for this specific download.

Operating mode description

BOOT	Operating mode	Comment
Leave open	Normal use	No download
Leave open	Download XMODEM	AT command for Download AT+WDWL
1*	Download specific	Need Wavecom PC software

For more information, see AT Commands Interface Guide for OS6.63 [14].

*See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

This BOOT pin must be left open for normal use or XMODEM download.

Pin description

Signal	Pin number	I/O	I/O type	Description
BOOT	12	I	1V8	Download mode selection

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3.10 Reset signal (~RESET)

This pin is tied to the internal reset pin of the Fastrack Supreme 10/20.

This signal is used to force a reset procedure by providing low level for at least 200µs. This signal must be considered as an emergency reset only. A reset procedure is already driven by the internal hardware during the power-up sequence.

This signal may also be used to provide a reset to an external device (at power up only). If no external reset is necessary, this input may be left open. If used (emergency reset), it must be driven by an open collector or an open drain.

The Fastrack Supreme 10/20 remains in reset mode as long as this ~RESET signal is held low.

Caution: This signal should only be used for "emergency" resets.

An Operating System reset is to be preferred to a hardware reset.

Reset sequence:

To activate the "emergency" reset sequence, the ~RESET signal has to be set to low for 200µs minimum. As soon as the reset is complete, the AT interface answers "OK" to the application.

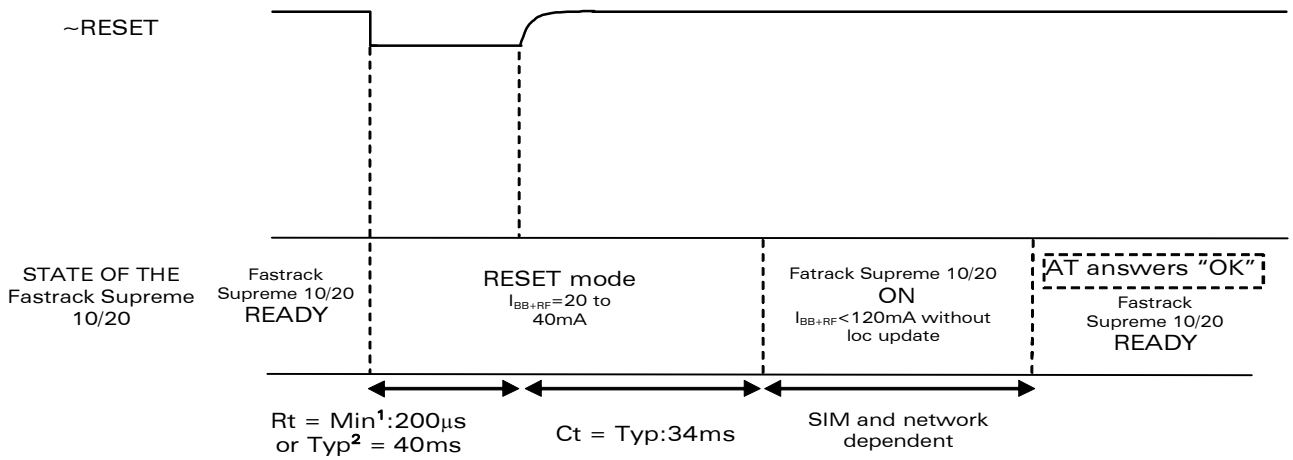

Figure 4: Reset Sequence Waveform

At power-up, the ~RESET time (Rt) is carried out after switching ON the Fastrack Supreme 10/20. It is generated by the internal voltage supervisor.

The ~RESET time is provided by the internal RC component. To keep the same time, it is not recommended to connect another R or C component on the ~RESET signal. Only a switch or an open drain gate is recommended.

Ct is the cancellation time required for Fastrack Supreme 10/20 initialization. Ct is automatically carried out by after hardware reset.

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Electrical characteristics of the signal

Parameter	Minimum	Typ	Maximum	Unit
Input Impedance (R)*		330K		Ω
Input Impedance (C)		10n		F
~RESET time (Rt) [1]	200			µs
~RESET time (Rt) [2] at power up only	20	40	100	ms
Cancellation time (Ct)		34		ms
V_H	0.57			V
V_{IL}	0		0.57	V
V_{IH}	1.33			V

* internal pull-up

* $V_{H:}$ Hysterisis Voltage

1 This reset time is the minimum to be carried out on the ~RESET signal when the power supply is already stabilized.

2 This reset time is internally carried out by the Fastrack Supreme 10/20 power supply supervisor only when the power supplies are powered ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
~RESET	13	I/O Open Drain	1V8	Fastrack Supreme 10/20 Reset

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3.11 External Interrupt

The Fastrack Supreme 10/20 provides one external interrupt input. This interrupt input can be activated on:

- **High** to **low** edge
- **Low** to **high** edge
- **Low** to **high** and **high** to **low** edge

When used, the interrupt input must not be left open.

If not used, this must be configured as GPIO.

Pin description

Signal	Pin number	I/O	I/O type	Reset state	Description	Multiplexed with
INT0	32	I	1V8	Z	External Interrupt	GPIO3

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

Electrical characteristics of the signals

Parameter		Minimum	Maximum	Unit
INT0	V_{IL}		0.54	V
	V_{IH}	1.33		V

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3.12 GSM-2V8 and GSM1V8 Output

These outputs must be used as a reference or as a pull-up resistor supply only. The voltage supplies are available when the Fastrack Supreme 10/20 is ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
GSM-2V8	11	O	Supply	Digital supply
GSM-1V8	10	O	Supply	Digital supply

Electrical characteristics of the signals

Parameter		Minimum	Typ	Maximum	Unit
GSM-2V8	Output voltage	2.74	2.8	2.86	V
	Output current			15	mA
GSM-1V8	Output voltage	1.76	1.8	1.94	V
	Output current			15	mA

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3.13 Digital Audio Interface (PCM)

Digital audio interface (PCM) allows connectivity with audio standard peripherals. It can be used for example to connect to an external audio codec.

The programmability of this mode allows to address a large range of audio peripherals.

PCM features:

- IOM-2 compatible device on physical level
- Master mode only with 6 slots by frame, user only on slot 0
- Bit rate single clock mode at 768KHz only
- 16 bits data word MSB first only
- Linear Law only (no compression law)
- Long Frame Synchronization only
- Push-pull configuration on PCM-OUT and PCM-IN

The digital audio interface configuration cannot differ from the above specified.

3.13.1 Description

The PCM interface consists of 4 wires:

- PCM-SYNC (output): The frame synchronization signal delivers an 8 KHz frequency pulse that synchronizes the frame data-IN and the frame data-OUT.
- PCM-CLK (output): The frame bit clock signal controls data transfer with the audio peripheral.
- PCM-OUT (output): The frame "data-OUT" relies on the selected configuration mode.
- PCM-IN (input): The frame "data-IN" relies on the selected configuration mode.

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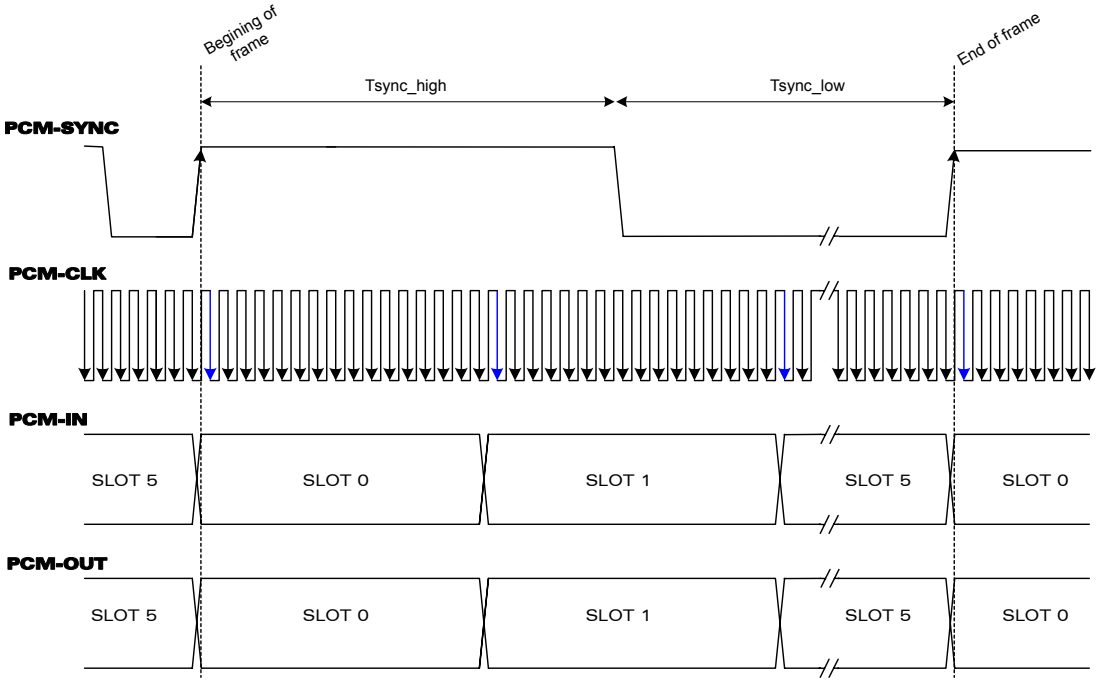

Figure 5: PCM frame waveform

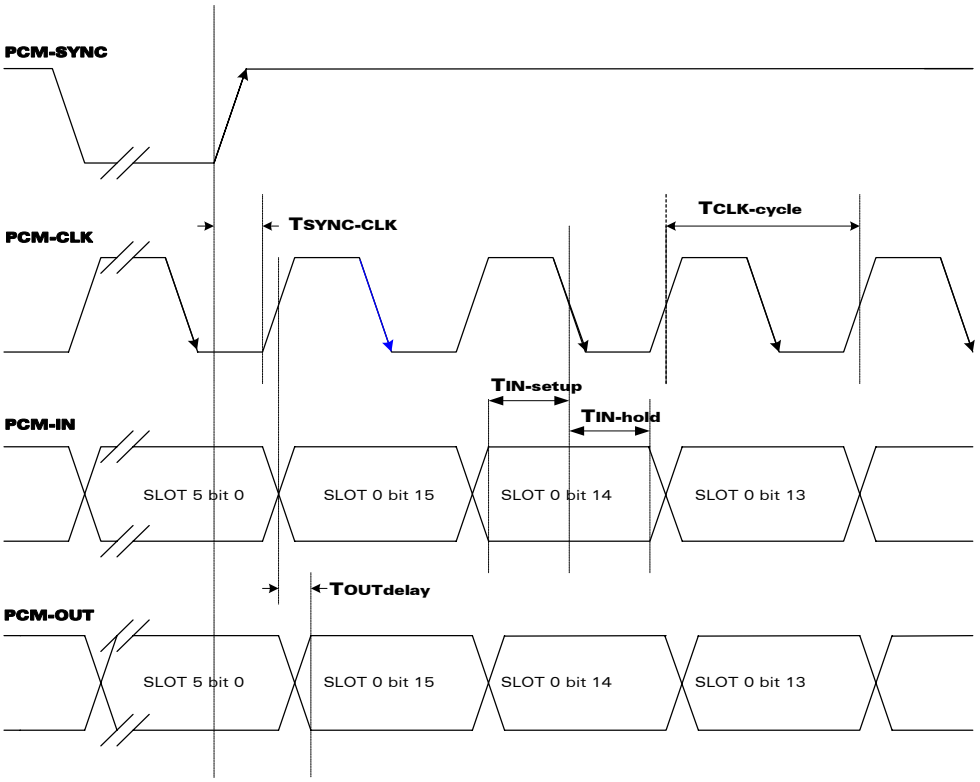

Figure 6: PCM sampling waveform

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AC characteristics

Signal	Description	Minimum	Typ	Maximum	Unit
$T_{sync\_low} + T_{sync\_high}$	PCM-SYNC period		125		µs
T_{sync_low}	PCM-SYNC low time		93		µs
T_{sync_high}	PCM-SYNC high time		32		µs
$T_{SYNC-CLK}$	PCM-SYNC to PCM-CLK time		-154		Ns
$T_{CLK-cycle}$	PCM-CLK period		1302		Ns
$T_{IN-setup}$	PCM-IN setup time	50			Ns
$T_{IN-hold}$	PCM-IN hold time	50			Ns
$T_{OUT-delay}$	PCM-OUT delay time			20	Ns

Pin description of the PCM interface

Signal	Pin number	I/O	I/O type	Reset state	Description
PCM-SYNC	36	O	1V8	Pull-down	Frame synchronization 8Khz
PCM-CLK	38	O	1V8	Pull-down	Data clock
PCM-OUT	39	O	1V8	Pull-up	Data output
PCM-IN	37	I	1V8	Pull-up	Data input

See Chapter 3.3, "Electrical information for digital I/O" for Open drain, 2V8 and 1V8 voltage characteristics and Reset state definition.

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3.14 USB 2.0 Interface

A 4-wire USB slave interface is available that complies with USB 2.0 protocol signaling. But it is not compliant with the electrical interface, due to the 5V of VPAD-USB.

The USB interface signals are VPAD-USB, USB-DP, USB-DM and GND.

USB interface features:

- 12Mbit/s full-speed transfer rate
- 3.3V typ compatible
- USB Softconnect feature
- Download feature is not supported by USB
- CDC 1.1 – ACM compliant

Note:

A 5V to 3.3V typ voltage regulator is needed between the external interface power in line (+5V) and the Fastrack Supreme 10/20 line (VPAD-USB).

Pin description of the USB interface

Signal	Pin number	I/O	I/O type	Description
VPAD-USB	7	I	VPAD_USB	USB Power Supply
USB-DP	8	I/O	VPAD_USB	Differential data interface positive
USB-DM	9	I/O	VPAD_USB	Differential data interface negative

Electrical characteristics of the signals

Parameter	Min	Typ	Max	Unit
VPAD-USB, USB-DP, USB-DM	3	3.3	3.6	V
VPAD_USB Current consumption		8		mA

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3.15 RF Interface

A space for MMCX connector is provided on the IESM board and the impedance is 50 Ω nominal. Depending on the application used this connector can be used either for GPS, Bluetooth or other types of RF devices.

3.15.1 External Active Antenna Specifications

If active antennas are used for example for GPS, typically a DC supply is applied through the RF connector.

The table below describes common characteristics of a GPS external antenna:

Antenna frequency range	1.57542GHz ± 1.023MHz (L1-Band)
Impedance	50 Ω nominal
Voltage Supply	3.3V ± 0.5VDC
Gain (antenna + cable)	2dBi (typical)

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4 Technical Specifications

4.1 General Purpose Connector Pin-out Description

Pin Number	Signal Name		Voltage	I/O*	Reset State	Description	Dealing with unused pins
	Nominal	Mux					
1	GND						
2	GND						
3	Reserve						
4	Reserve						
5	Reserve						
6	Reserve						
7	VPAD-USB		VPAD-USB	I		USB Power supply input	NC
8	USB-DP		VPAD-USB	I/O		USB Data	NC
9	USB-DM		VPAD-USB	I/O		USB Data	NC
10	GSM-1V8		1V8	O		1.8V Supply Output	NC
11	GSM-2V8		2V8	O		2.8V Supply Output	NC
12	BOOT		1V8	I		Boot Input	NC
13	~RESET		1V8	I/O		RESET Input	NC
14	AUX-ADC		Analog	I		Analog to Digital Input	NC or Pull to GND
15	~SPI1-CS	GPIO31	2V8	O	Z	SPI1 Chip Select	NC
16	SPI1-CLK	GPIO28	2V8	O	Z	SPI1 Clock	NC
17	SPI1-I	GPIO30	2V8	I	Z	SPI1 Data Input	NC
18	SPI1-IO	GPIO29	2V8	I/O	Z	SPI1 Data Input / Output	NC
19	SPI2-CLK	GPIO32	2V8	O	Z	SPI2 Clock	NC
20	SPI2-IO	GPIO33	2V8	I/O	Z	SPI2 Data Input / Output	NC
21	~SPI2-CS	GPIO35	2V8	O	Z	SPI2 Chip Select	NC
22	SPI2-I	GPIO34	2V8	I	Z	SPI2 Data Input	NC
23	CT104-RXD2	GPIO15	1V8	O	Z	Auxiliary RS232 Receive	Add a test point for debugging

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24	CT103-TXD2	GPIO14	1V8	I	Z	Auxiliary RS232 Transmit	**(TXD2) Pull-up** to VCC_1V8 with 100kΩ and add a test point for debugging
25	~CT106-CTS2	GPIO16	1V8	O	Z	Auxiliary RS232 Clear To Send	**(CTS2)** Add a test point for debugging
26	~CT105-RTS2	GPIO17	1V8	I	Z	Auxiliary RS232 Request To Send	**(RTS2) Pull-up** to VCC_1V8 with 100kΩ and add a test point for debugging
27	GPIO8		1V8	I/O	Pull-up		NC
28	GPIO26	SCL	Open Drain	O	Z	I²C Clock	NC
29	GPIO19		2V8	I/O	Z		NC
30	GPIO27	SDA	Open Drain	I/O	Z	I²C Data	NC
31	GPIO20		2V8	I/O	Undefined		NC
32	INT0	GPIO3	1V8	I	Z	Interruption 0 Input	If INT0 is not used, it should be configured as GPIO
33	GPIO23	*	2V8	I/O	Z		NC
34	GPIO22	*	2V8	I/O	Z		NC
35	~CT108-2-DTR1	GPIO41	2V8	I	Z	Main RS232 Data Terminal Ready	**(DTR1) Pull-up** to VCC_2V8 with 100kΩ
36	PCM-SYNC		1V8	O	Pull-down	PCM Frame Synchro	NC
37	PCM-IN		1V8	I	Pull-up	PCM Data Input	NC
38	PCM-CLK		1V8	O	Pull-down	PCM Clock	NC
39	PCM-OUT		1V8	O	Pull-up	PCM Data Output	NC
40	AUX-DAC		Analog	O		Digital to Analog Output	NC
41	VCC-2V8		2V8	O		Power Supply	
42	GND		GND			GND	
43	DC-IN IESM		5V5-32V	O		Power Supply	
44	DC-IN IESM		5V5-32V	O		Power Supply	
45	GND		GND			GND	
46	4V		4V	O		Power Supply	
47	4V		4V	O		Power Supply	
48	GND		GND			GND	
49	GND		GND			GND	
50	GND		GND			GND	

* For more information about the multiplexing of these signals, see “General purpose input /output”, Chapter 3.6

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4.2 Environmental Specifications

The Fastrack Supreme 10/20 is compliant with the following operating class. To ensure the proper operation of the IESM, the temperature of the environment must be within a specific range as described in the table below:

Fastrack Supreme without IESM	
Conditions	Temperature range
Operating / Class A	-20°C to +55°C
Operating / Class B	**-30°C to +75°C**
Storage	-40°C to +85°C

Fastrack Supreme with IESM	
Conditions	Temperature range
Operating / Class A	-20°C to +55°C
Operating / Class B	**-30°C to +65°C**
Storage	-40°C to +85°C

Function Status Classification:

Class A:

The Fastrack Supreme 10/20 and the IESM remains fully functional, meeting GSM performance criteria in accordance with ETSI requirements, across the specified temperature range.

Class B:

The Fastrack Supreme 10/20 and the IESM remains fully functional, across the specified temperature range. Some GSM parameters may occasionally deviate from the ETSI specified requirements and this deviation does not affect the ability of the Wireless CPU® to connect to the cellular network and to be fully functional.

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The detailed climatic and mechanics standard environmental constraints applicable to the Fastrack Supreme 10/20 are listed in the table below:

Q2687		ENVIRONNEMENTAL CLASSES		
TYPE OF TEST	STANDARDS	STORAGE Class 1.2	TRANSPORTATION Class 2.3	OPERATING (PORT USE) Class 7.3
Cold	IEC 68-2.1 Ab test	-25° C 72 h	-40° C 72 h	-20° C (GSM900) 16 h -10° C (GSM1800/1900) 16h
Dry heat	IEC 68-2.2 Bb test	+70° C 72 h	+70° C 72 h	+55° C 16 h
Change of temperature	IEC 68-2.14 Na/Nb test		-40° / +30° C 5 cycles t1 = 3 h	-20° / +30° C (GSM900) 3 cycles -10° / +30° C (GSM1800/1900): 3 cycles t1 = 3 h
Damp heat cyclic	IEC 68-2.30 Db test	+30° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1
Damp heat	IEC 68-2.56 Cb test	+30° C 4 days	+40° C 4 days	+40° C 4 days
Sinusoidal vibration	IEC 68-2.6 Fc test	5 - 62 Hz : 5 mm / s 62 - 200Hz : 2 m / s2 3 x 5 sweep cycles		
Random vibration wide band	IEC 68-3.36 Fdb test		5 - 20 Hz : 0.96 m2 / s3 20 - 500Hz : - 3 dB / oct 3 x 10 min	10 -12 Hz : 0.96 m2 / s3 12 - 150Hz : - 3 dB / oct 3 x 30 min

Figure 7: Environmental classes

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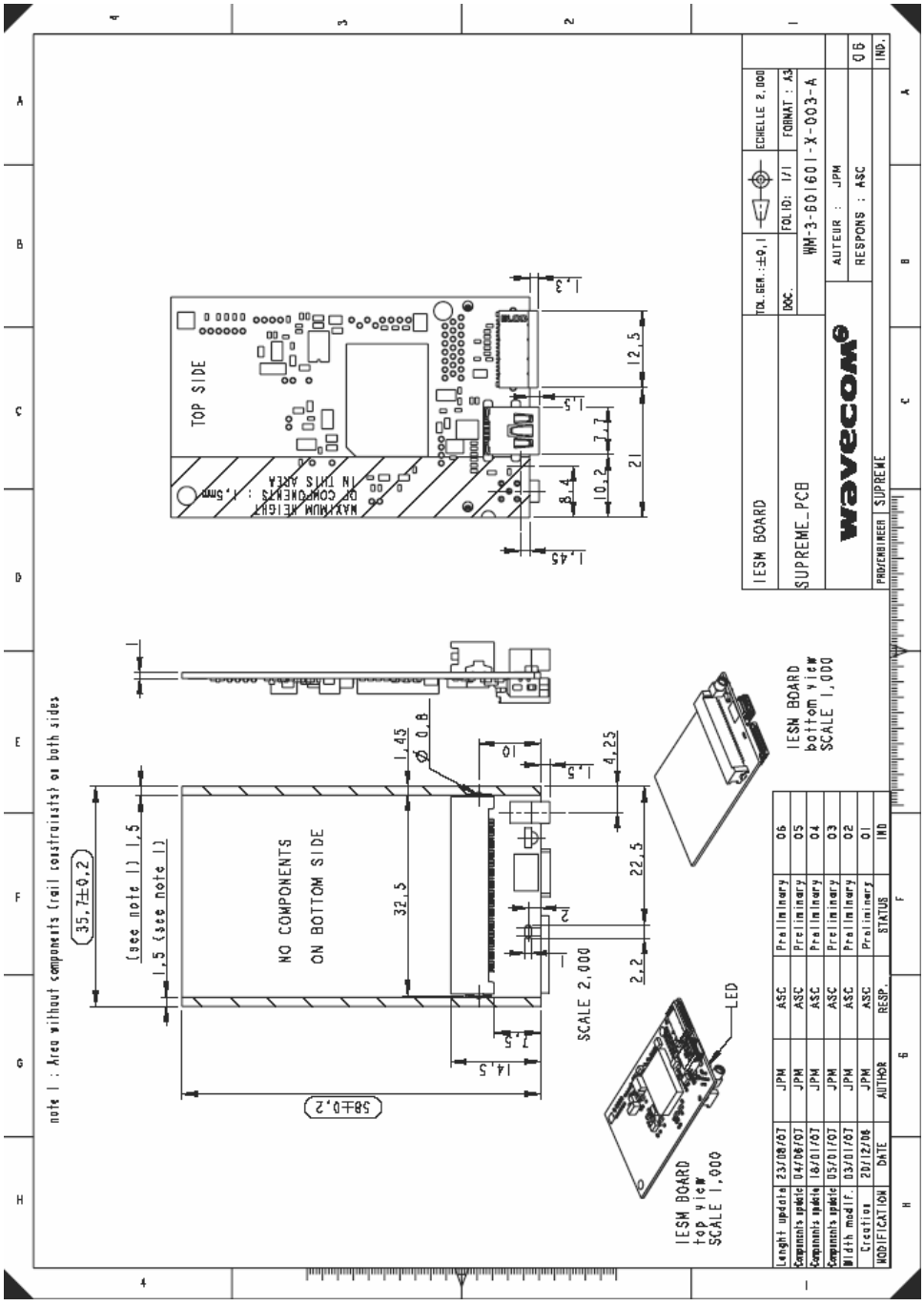
4.3 Mechanical Specifications

4.3.1 IESM PCB Mechanical Drawings



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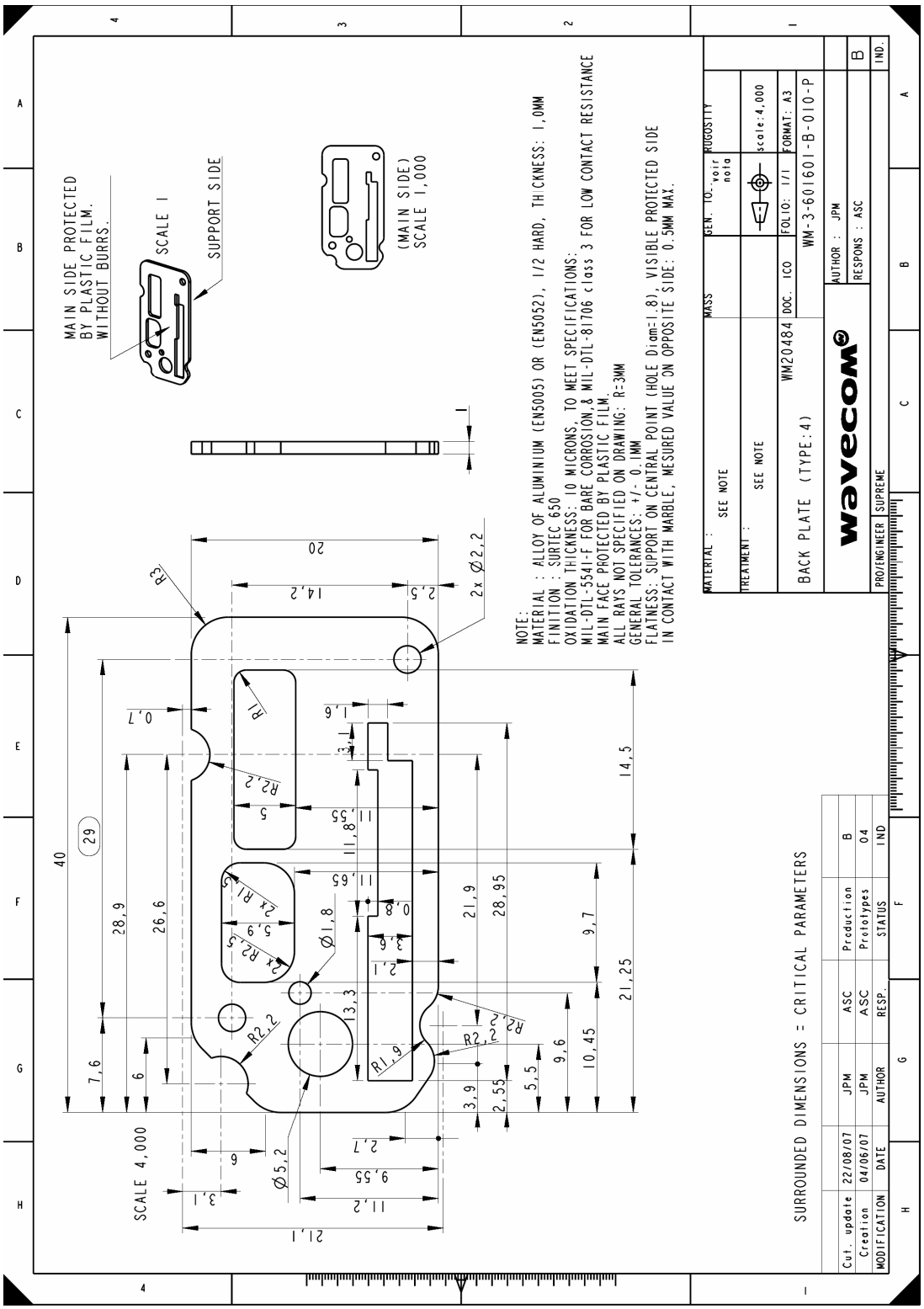
4.3.2 IESM Back Plate Mechanical Drawings



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5 Connector and Peripheral Devices References

5.1 General Purpose Connector References

GPC is a 50-pin plug connector with 0.5mm pitch from Kyocera Elco:

14 5078 050 515 861+ (IESM side)

GPC is a 50-pin connector Matting connector

24 5078 050 513 861+ (Fastrack Supreme 10/20 side)

16 Way I/O Socket with 0.625mm pitch from Kyocera Elco:

20 9257 016 001 013 (IESM side)

16 Way I/O plug with 0.625mm pitch from Kyocera Elco:

58-9257-000-000-012S

Mini USB connector with 0.8mm pitch from Molex:

54819-0572 (IESM side)

For further details, see the data sheets in the Appendix. More information is also available from;

http://www.avxcorp.com/

http://www.molex.com/

5.2 RF Connector

MMCX Connector from Amphenol:

MMCX6252N3-3GT30G-50 (IESM side)

For further details, see the data sheets in the Appendix. More information is also available from;

http://www.amphenol.com

5.3 GPS Antenna

GPS antennas and support for antenna adaptation can be obtained from manufacturers such as:

- http://www.mitsumi.com/
- http://www.wi-sys.com/
- http://www.tokoam.com/

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6 Design Guidelines

6.1 Hardware and RF

6.1.1 Conformity

The Fastrack Supreme 10/20 product complies with the essential requirements of article 3 of R&TTE 1999/5/EC Directive and satisfied the following standards.

Domain	Applicable standard
Safety standard	EN 60950 (ed.1999)
Efficient use of the radio frequency spectrum	EN 301 419-(v 4.1.1) EN 301 511 (V 7.0.1)
EMC	EN 301 489–1 (edition 2002) EN 301 489-7 (edition 2002)
Global Certification Forum – Certification Criteria	GCF-CC V3.13.0
FCC	FCC Part 15 FCC Part 22, 24
IC	RSS-132 Issue 2 RSS-133 Issue 3

Important:

Fastrack Supreme 10/20 complies with the essential requirements as described above. Customer designed IESM when used with Fastrack Supreme 10/20 may require additional certification in order for the whole product to be fully compliant.

6.1.2 EMC Recommendations

The EMC tests must be performed on the application as soon as possible to detect any potential problems.

When designing, special attention should be paid to:

- Possible spurious emission radiated by the application to the RF receiver in the receiver band

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- ESD protection **is mandatory** on all signals which have external accessibility (typically human accessibility).
    - Typically, ESD protection is mandatory for the:
        - IO Expander Connector
        - USB
- Ground plane: Wavecom recommends a common ground plane for analog/digital/RF grounds and the IESM board must be properly grounded with Fastrack Supreme metallic housing.

Important:

In order for the IESM board to have the best grounding, Wavecom recommends to attach the ground plane of the PCB to the back plate and not to the Fastrack Supreme main housing. Wavecom designed IESM's achieved this by using a metallic spring that attaches to the USB opening of the back plate.

It is important to note if customer wishes to build their own IESM's without the USB option, they must find a way to properly ground the IESM to the back plate of the Fastrack Supreme.

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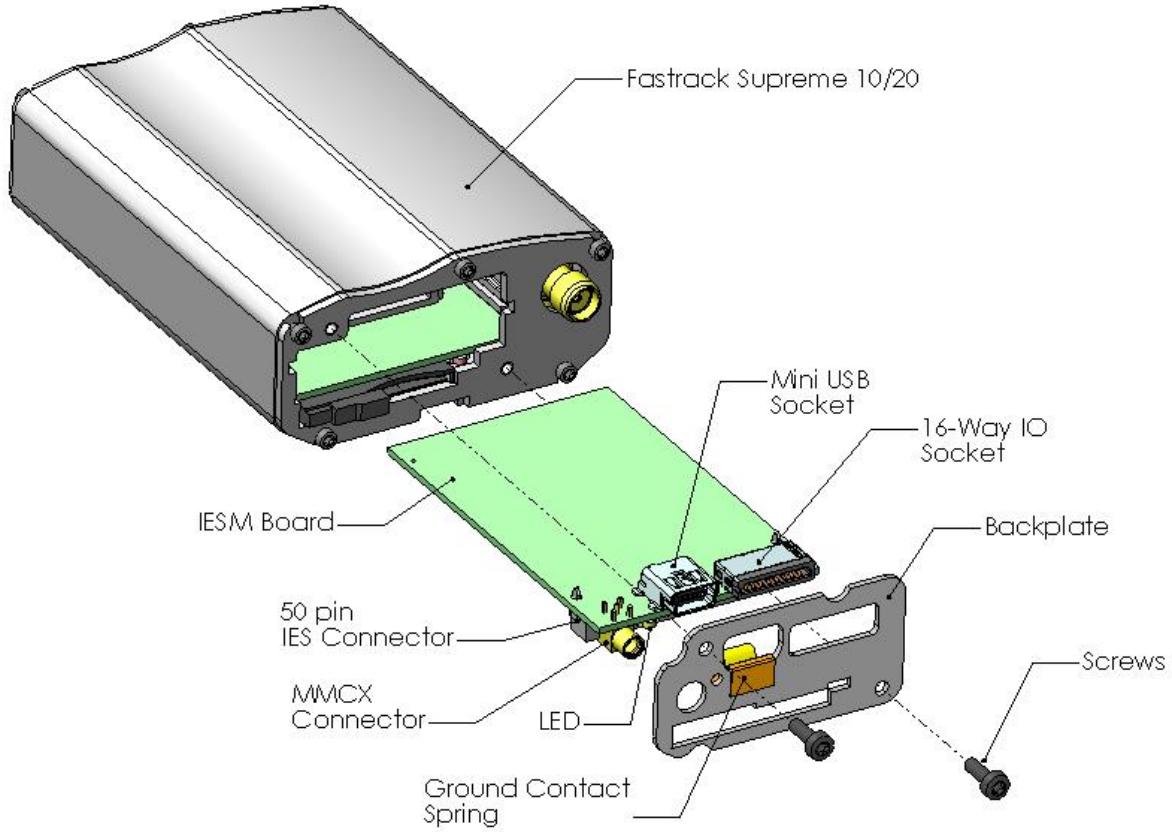
6.2 Mechanical Integration



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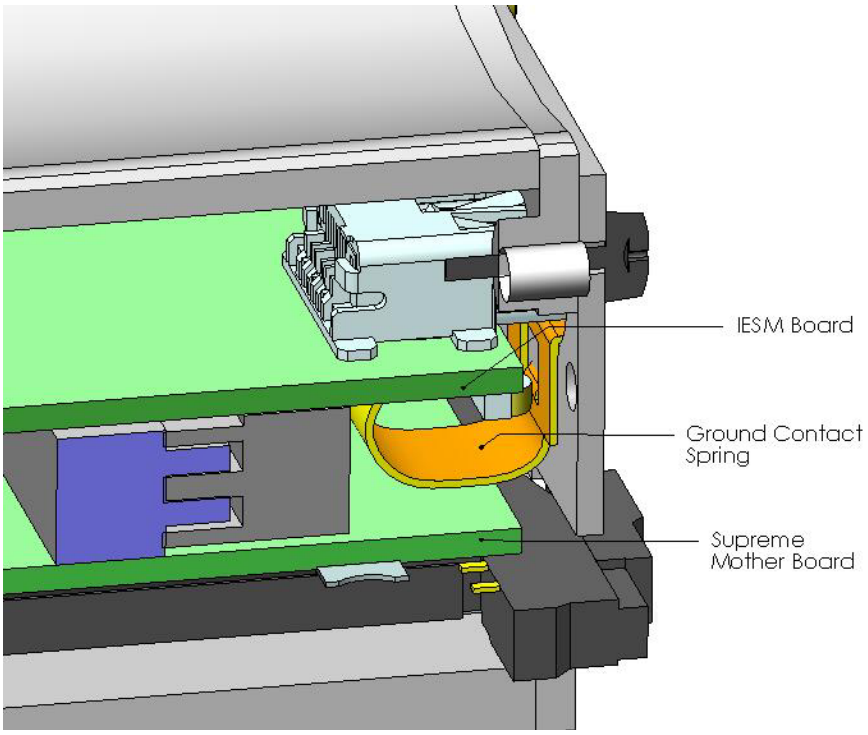

Important:

Best grounding for IESM is utilized by using a ground spring contact that attaches to the USB opening of the back plate.

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7 Appendix

7.1 Connector Reference Documents

Reference technical specifications of the connectors for the IESM are shown below:

Molex
548190572_sd.pdf

Amphenol
RNT89976_01.pdf

AVX
14-5078-050-515-86:

AVX
20-9257-01-000S.pdf

7.2 Back Plates Reference

There are 4 types of back plates available to suit different IESM board usage, depending on the type of connectors being used on the IESM board.

Back Plate	WM Code	Opening for			
		MMCX	LED	USB	16-pin I/O connector
Type 1	WM20197	X	X	X	X
Type 2	WM20480	YES	YES	YES	X
Type 3	WM20482	X	X	YES	YES
Type 4	WM20484	YES	YES	YES	YES

7.3 Extraction Tool Reference

There is an extraction tool which can help removing the IESM board from the Fastrack Supreme Plug & Play.

WM20411.pdf

A hole is required on the IESM board with dimension of 1 x 2.2mm oval hole. For detail, please refer to Section 4.3.1 for possible positioning.

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8 Safety Recommendations (For Information Only)

IMPORTANT

FOR THE EFFICIENT AND SAFE OPERATION OF YOUR GSM APPLICATION BASED ON Fastrack Supreme 10/20

PLEASE READ THIS INFORMATION CAREFULLY

8.1.1 RF Safety

8.1.1.1 General

Your GSM terminal[1] is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out and receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

8.1.1.2 Exposure to RF Energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was fitted for use.

If you are concerned about exposure to RF energy, there are things you can do to minimize exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines below:

8.1.1.3 Efficient Terminal Operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However, your GSM terminal operates more efficiently with the antenna when fully extended.

1 Based on Wireless CPU® Quik Q2687

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Do not hold the antenna when the terminal is "IN USE". Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

8.1.1.4 Antenna Care and Replacement

Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. Consult your manual to see if you may change the antenna to yourself. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.

Use only the supplied or approved antenna. Unauthorized antennas, modifications or attachments could damage the terminal and may contravene local RF emission regulations or invalidate type approval.

8.1.2 General Safety

8.1.2.1 Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please:

- give full attention to driving,
- pull-off the road and park before making or answering a call if driving conditions so require.

8.1.2.2 Electronic Devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However, RF energy may affect some improperly shielded electronic equipment.

8.1.2.3 Vehicle Electronic Equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

8.1.2.4 Medical Electronic Equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal OFF in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

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8.1.2.5 Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you to have permission from a crew member to use your terminal while the aircraft is on the ground. To prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

8.1.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

8.1.2.7 Blasting Areas

To avoid interfering with blasting operations, turn your unit OFF when in a "blasting area" or in areas posted: "turn off two-way radio". Construction crew often uses remote control RF devices to set off explosives.

8.1.2.8 Potentially Explosive Atmospheres

Turn your terminal OFF when you are in any area with a potentially explosive atmosphere. Though it is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations; below decks on boats; fuel or chemical transfer or storage facilities; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is to be used.

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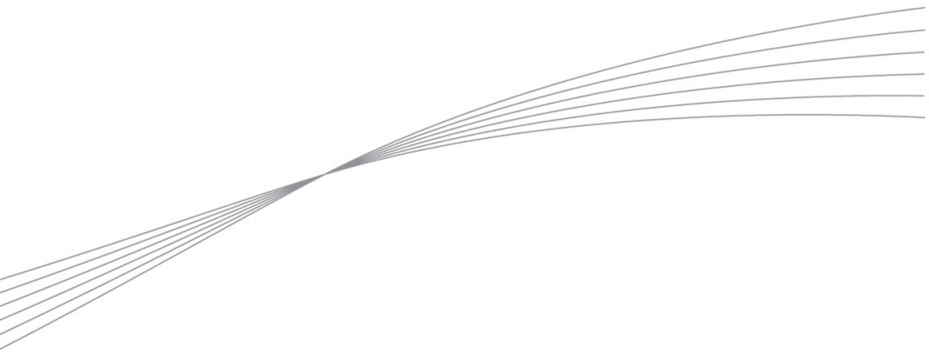

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Make it wireless

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