Product Datasheet

ePR1015B

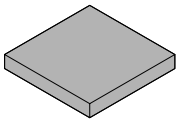
Prelude One

Fully Integrated GPS RF Receiver

■ GENERAL DESCRIPTION

The ***Prelude One*** RF Receiver *(*ePR1015B) implements a LNA, an image-reject mixer with a RF-AMP, a band pass filter, an AGC, and a fully integrated VCO/PLL. The mixer down-converts to a fixed IF of 3.564MHz, the AGC controlled IF signal is quantized with 2-bit (SIGN / MAG) outputs. A 27.456MHz reference signal is used for LO generation and CLKOUT.

The ***Prelude One*** IC reduces external components to minimize the bill of material and the size of board area.



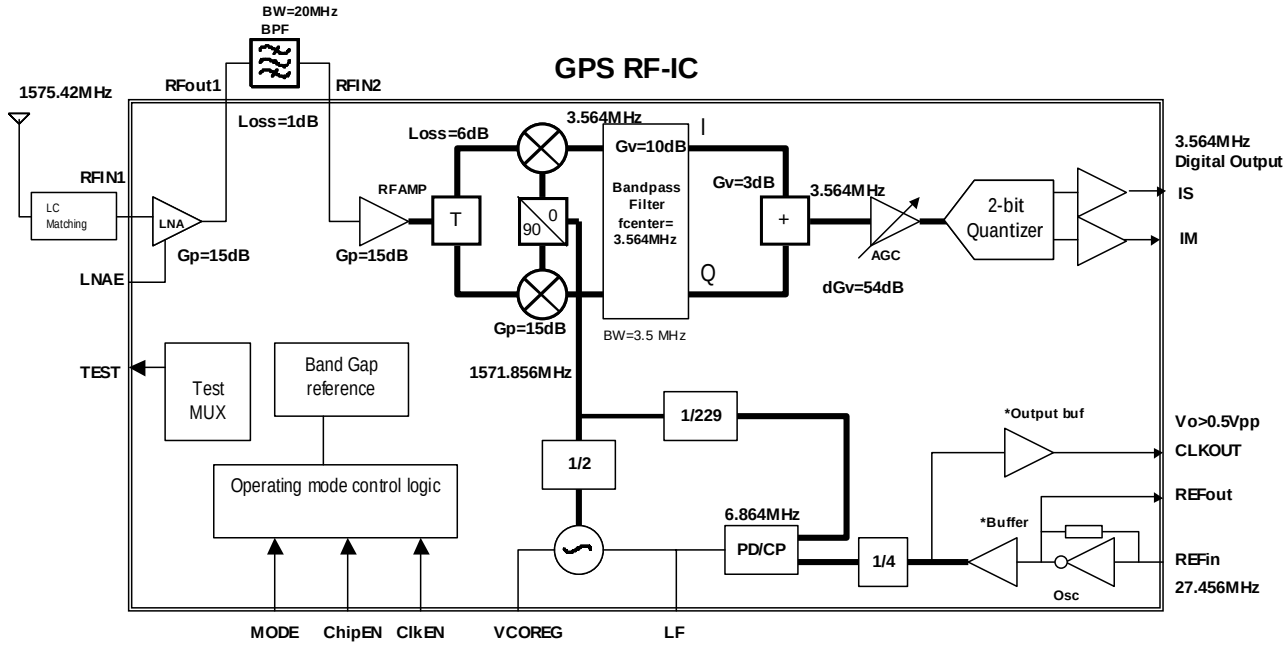
(LCC-32P-M08)

LCC-32P-M08

■ FEATURES

- Supports GPS L-band C/A code.
- Single conversion architecture with on-chip IF-filter.
- 2-bit (SIGN /MAG) digital output
- Low supply current 31.5mA / 1.5mA / 1uA in Operation / Stand-by / Sleep mode.
- On-chip fully integrated VCO
- Fully integrated LO generator
- Low supply voltage down to 2.7V
- Operating temperature range: -40° to +85℃
- Package: Very small BCC-32 (5mm x 5mm)

■ BLOCK DIAGRAM



BLOCK DESCRIPTION

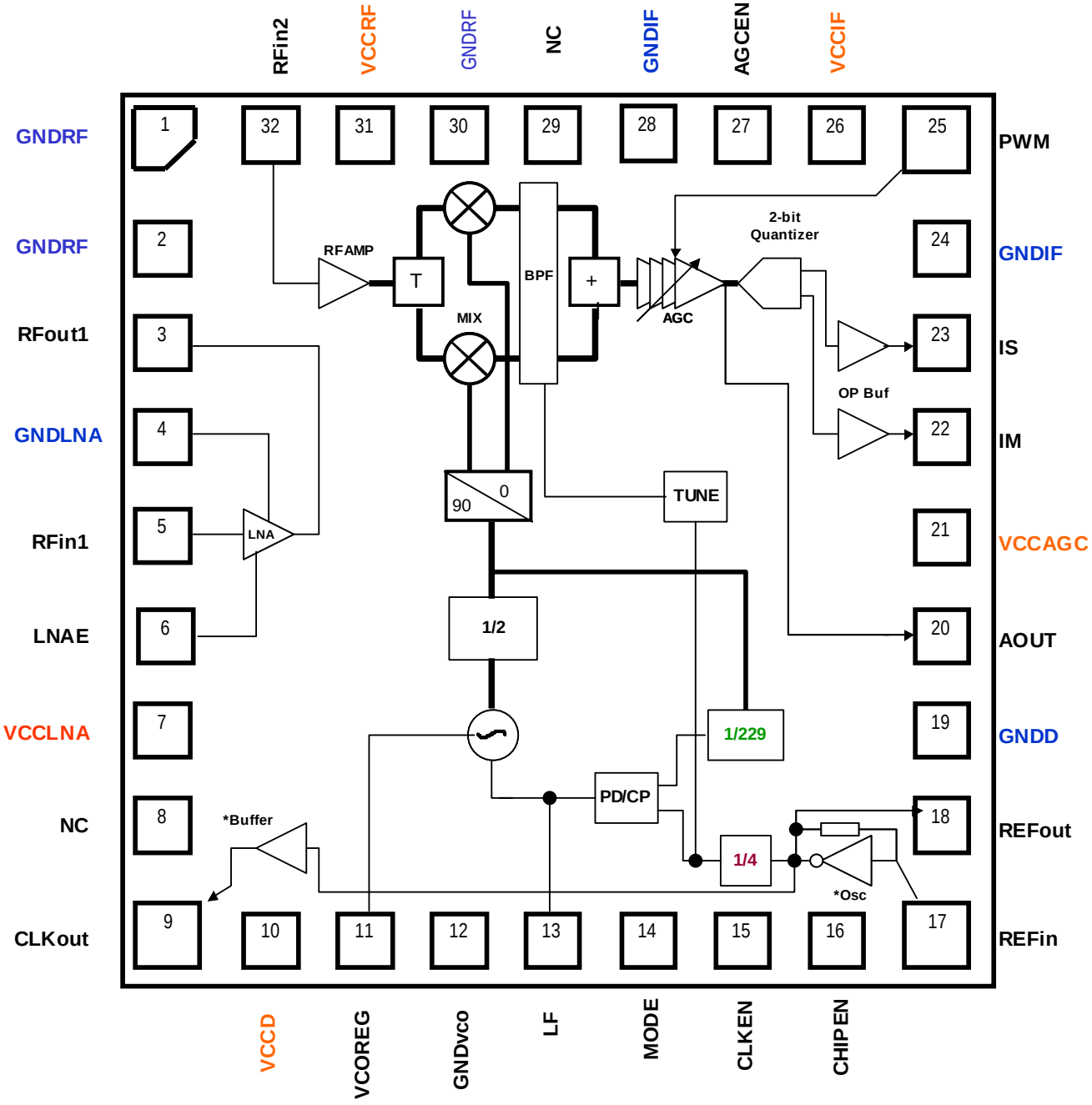
- **Receiver Block**

The receiver consists of a LNA, an image-reject mixer with a RF-AMP, a band pass filter, an AGC IF amplifier, CLK output buffer, fully integrated VCO and a PLL, which generates a local signal for the down mixers with a 27.456MHz reference signal. The down mixers convert a RF signal to a fixed IF frequency of 3.564MHz.

A list of functional blocks:

- **LNA**
- **RF-AMP**
- **Image Reject Mixer**
- **Down converting Mixers**
- **IF filter**
- **Summing Amplifier**
- **IF-AMP (PGA) with AGC (optional external control)**
- **2 Bit Quantizer of IF signal (Sign/Magnitude)**
- **Local Oscillator (PLL)**
- **Fully integrated VCO**
- **TCXO input buffer**
- **CLK output buffer**

■ PIN ASSIGNMENT AND FLOOR PLAN



This target specification is the design specification for product development. After more examination is done, this target may change

Pin Description

Pin No.	Name	Description
1	GNDRF	Ground for the RFAMP, MIXER, IF-BPF.
2	GNDRF	Ground for the RFAMP, MIXER, IF-BPF.
3	RFout1	LNA output.
4	GNDLNA	Ground for the LNA.
5	RFin1	LNA input.
6	LNAE	Emitter port of the LNA. Common emitter connection.
7	VCCLNA	Power supply for the LNA
8	NC	Not connected
9	CLKout	Clock 27.456 MHz output. “H” when ChipEN and ClkEN are “L”, see table 1.
10	VCCD	Power supply for the dividers and CMOS in/output buffers.
11	VCOREG	Pin for the regulated voltage for the VCO. Connect a grounded capacitor for noise filtering.
12	GNDvco	Ground for the VCO
13	LF/REFR	PLL Loop Filter / CP current setting R, depending on version
14	MODE	Connect to VCC
15	ClkEN	Enable Clock buffer and CLKout. CMOS input. See table 1.
16	ChipEN	Enable all components on chip. CMOS input. See table 1.
17	REFin	Input for an external reference clock of 27.456 MHz TCXO. Use AC connection.
18	REFout	Output of reference frequency buffer, for use with XTO.
19	GNDD	Ground for the divider and CMOS in/output buffers.
20	AOUT	Analog IF output. Use low capacitive probe.
21	VCCAGC	Power supply for AGC circuit.
22	IM	Magnitude bit of 3.564 MHz IF signal output. (low: |x|<thresh). “L” when ChipEN is “L”, see table 1.
23	IS	Sign bit of 3.564 MHz IF signal output. (low: x>0). “L” when ChipEN is “L”, see table 1.
24	GNDIF	Ground for the IF-AMP (AGC).
25	PWM	Gain control input for the IF-AGC. <1V: max gain, >2.3V: min gain. Connect 100nF capacitor to GND to integrate AGC_CP current.
26	VCCIF	Power supply for the IF-AMP (AGC).
27	AGCEN	Connect to GND
28	GNDIF	Ground for the IF-AMP (AGC).
29	NC	Not connected
30	GNDRF	Ground for the RFAMP, MIXER, IF-BPF.
31	VCCRF	Power supply for the RFAMP, MIXER, IF-BPF.
32	Rfin2	Input of the RF-AMP

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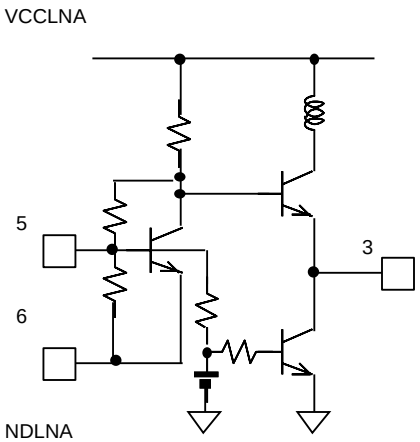
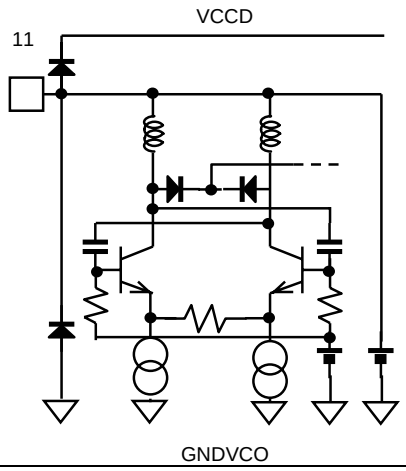
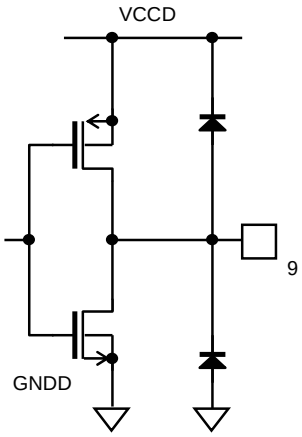
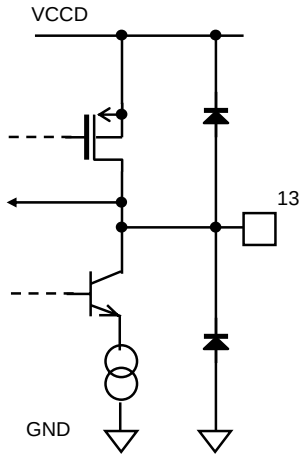
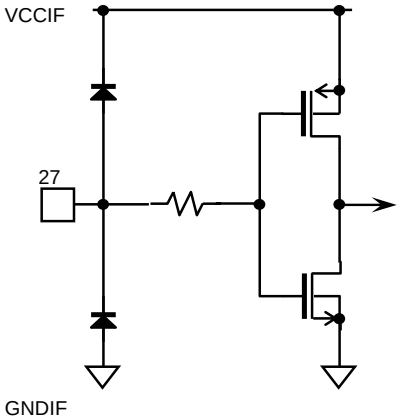
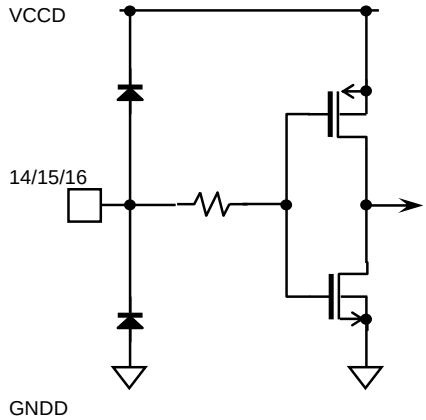
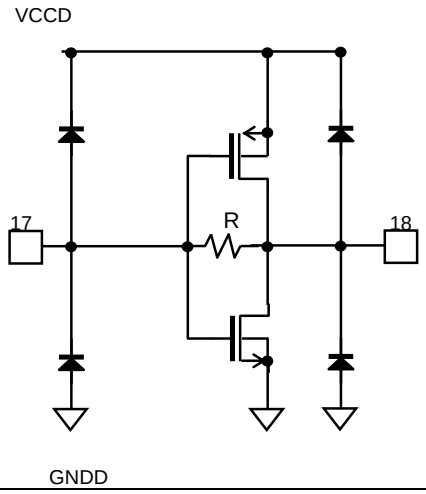
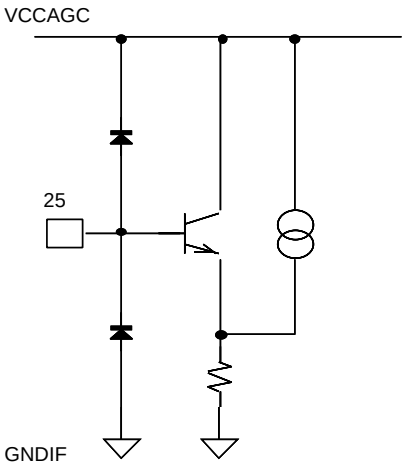
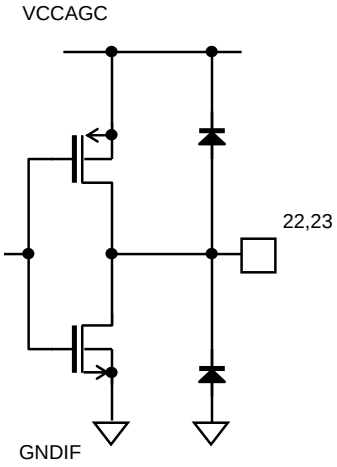
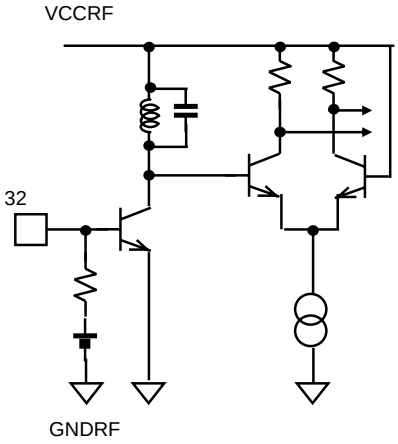
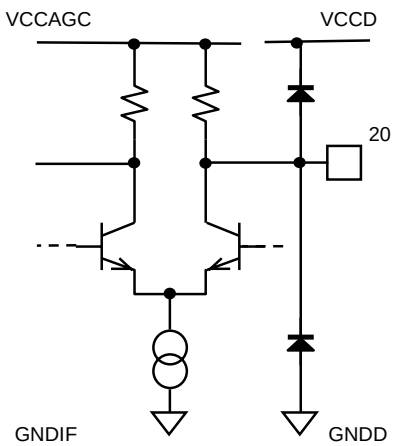
Input/Output Equivalent Circuits

	Pin name	Equivalent Circuit		Pin name	Equivalent Circuit
3 5 6	Rfout1 RFin1 LNAE		11 12	VCOREG GNDVCO	
9	CLKOUT		13	LF	
27	AGCEN (no function)		14 15 16	MODE CLKEN CHIPEN	

(continued)

	Pin Name	Equivalent Circuit		Pin name	Equivalent Circuit
17 18	REFIN REFout		25	PWM	
22 23	IM IS		32	RFin2	

	Pin name	Equivalent Circuit		Pin name	Equivalent Circuit
20	AOUT				

■ ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{CC}	-0.5 to +4.0	V	
Maximum power supply voltage.	V_X	$V_{CC} < V_X < 4.0$	V	Open is prohibited, when voltages are supplied on other pins.
Input voltage	V_I	–0.5 to VCC +0.5	V	
Output voltage	V_O	–0.5 to VCC +0.5	V	
Output current	I_O	0 to 10	mA	
Storage temperature	T_{stg}	-55 to +125[*1]	°C	

Note: - Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.3	V	
Input voltage	V_I	GND	-	V_{CC}	V	
Ambient temperature	T_A	-40		+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

[DC Characteristics] (Vcc=3.0V, Ta=25°C)

Parameter		Symbol	Target Value			Unit	Notes
			Min.	Typ.	Max.		
Power supply current	Total RX	Icc		31.5		mA	With REFin signal (27.456MHz)
Standby supply current	Stand-by	I_{std}		1.5	2.5	mA	OSC input buffer and CLKout output buffer are activated
Sleep current	Sleep	I_{sleep}		1	10	μA	Sleep mode (10μA tested in factory)
"H" level Input voltage.	MODE, ClkEN, ChipEN	VIH	Vcc × 0.7+0.4	-	-	V	CMOS Digital input pins
"L" level Input voltage.		VIL	-	-	Vcc x 0.3 –0.4	V	CMOS Digital input pins
"H" level Input current.	MODE, ClkEN, ChipEN	IIH	-1.0	-	+1.0	μA	CMOS Digital input pins
"L" level Input current.		IIL	-1.0	-	+1.0	μA	CMOS Digital input pins
"H" level output voltage.	IS, IM	VOH	Vcc –0.4	-	-	V	Digital output pins, I_{OL}=-1mA
"L" level output voltage.		VOL	-	-	0.4	V	Digital output pins, I_{OH}=1mA
"H" level output current.	IS, IM	IOH	-1.0	-	-	mA	Digital output pins, Vcc=3V
"L" level output current.		IOL	-	-	1.0	mA	Digital output pins, Vcc=3V.

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[AC Characteristics] (Vcc=3.0V, Ta=25°C)

Parameter	Symbol	Target Value			Unit	Notes
		Min.	Typ.	Max.		
Receiver Characteristics						
Receiver input frequency	f_{RX}		1575.420		MHz	Half of VCO oscillating frequency
Local frequency	f_{LO}		1571.856		MHz	
IF output frequency	f_{OUT}		3.564		MHz	
Reference clock frequency	f_{OSC}		27.456		MHz	TCXO or XTO (option)
Overall Receiver Gain	G_{v3}		77		dB	@AOUT for AGC min. gain
	G_{v4}		110		dB	@AOUT for AGC max. gain Pin=-120dBm
Overall Noise Figure	NF		3.8		dB	Measured at LNA input Pin=-120dBm.
Blocking Immunity	Block		(TBD)			See blocking profile in appendix
Blocking signal level	P_{BLOCK}			-75	dBm	Measured at LNA input.
Local signal leak level	P_{LOLEAK}			-65	dBm	Measured at LNA input.
Image suppression	IR	15	23		dB	
RF ports Input/Output impedance	Zin/Zout		50		Ω	RFin1, Rfout1, RFin2 pins
Receiver turn-ON time	T_{LOCKUP}		-	10	ms	VCO/PLL wake-up time from stand-by mode.
	T_{setAGC}		-	10	ms	Settling time of the AGC

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[AC Characteristics, contd.] (Vcc=3.0V, Ta=25°C)

Parameter	Symbol	Target Value			Unit	Notes
		Min.	Typ.	Max.		
LNA						
Operating frequency	f_{RF}		1575.42		MHz	
Power gain	G_P	12	15	18	dB	
Noise figure	NF		1.6	2.2	dB	RS=50Ω
1dB compression point	IP1dB		-30		dBm	Measured at LNA input
3rd order intercept point	IIP3		-20		dBm	Measured at LNA input
Input VSWR	VSWR			2	-	Measured at LNA input, 50-ohm, includes output matching network
Output VSWR	VSWR			2	-	Measured at LNA output, 50-ohm, includes output matching network
RFAMP						
Operating frequency	f_{RF}		1575.42		MHz	
Power gain	G_P		(15)		dB	
Noise figure	NF		(2.3)	(3.0)	dB	
1dB compression point	IP1dB		(-30)		dBm	Measured at RFAMP input
3rd order intercept point	IIP3		(-20)		dBm	Measured at RFAMP input
Input VSWR	VSWR			2	-	Measured at RFAMP input, 50-ohm, RFAMP includes input and output matching network
Power splitter						
Insertion loss	IL		(6)		dB	
Input Return loss	NF		(6)		dB	
Image Reject Down-converting Mixer						
Operating Frequency	f_{RF}		1575.420		MHz	
	f_{LO}		1571.856		MHz	Low-side injection
	f_{IF}		3.564		MHz	
Conversion Gain	G_C		(15)		dB	
SSB Noise figure	NF_{SSB}		(10)	(12)	dB	
1dB compression point	IP1dB		(-36)		dBm	
Input IP3	IIP3		(-26)		dBm	

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[AC Characteristics, contd.] (Vcc=3.0V, Ta=25°C)

Parameter	Symbol	Target Value			Unit	Notes
		Min.	Typ.	Max.		
Band-pass Filter (Complex filter)						
Pass band center frequency	f_{CENTER}		3.564		MHz	
3dB band width	BW_{3dB}	2.8	3.5	4	MHz	f_{CENTER}=3.564MHz (actual requirements will be based on system measurements)
Stop band	SB_{30MHz}	55			dB	At f_{CENTER}=+30MHz
Gain	G		(10)		dB	Within pass band
Maximum input level	V_{MAX}	(40)			mVpp	Corresponds to -24dBm into 50Ω
Group delay	GD		(300)		nsec	Within pass band
Ripple	Rip		TBD		dB	Within pass band
Summing						
Gain	G		(3)		dB	
IF-AMP						
Operating frequency	f_{IF}		3.564		MHz	
Gain	G_H		(28)		dB	@High gain setting MODE="H"
	G_L		(4)		dB	@Low gain setting MODE="L"
Noise figure	NF_L		(27)		dB	@Low gain setting at 800 Ohm diff.
Noise figure	NF_H		(10)		dB	@High gain setting at 800 Ohm diff.
IF-AGC						
Operating frequency	f_{IF}		3.564		MHz	
Gain	Gvmin		14		dB	V(PWM) > xx V
	Gvmax		68		dB	V(PWM) < xx V
Gain control range	DGL	35			dB	
Control Voltage vs. AGC gain			(TBD)			See appendix for the Gain slope.
AGC response time	t_{AGC}			10	msec	(Vo =+/- 2dB)
AOUT Output voltage	V_o		0.8		Vpp	(for test only)
2-Bit IF ADC						
Magnitude bit		"L": |x|<thresh	3.564 MHz IF signal			
Sign bit		"L": x>0	3.564 MHz IF signal			
AGC Control						
Average duty cycle of IM bit	Mduty	30		46	%	
Average duty cycle of IS bit	Sduty	42		58	%	

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[AC Characteristics, contd.] (Vcc=3.0V, Ta=25°C)

Parameter	Symbol	Target Value			Unit	Notes
		Min.	Typ.	Max.		
VCO & 0/90 degrees phase shifting divider						
Oscillation frequency	f_{VCO}		3143.712		MHz	fLO*2, PLL in lock
Phase Noise	C/N1			(-65)	dBc/Hz	At divider output Δf=1kHz, BW=1Hz, PLL in lock
	C/N2			(-120)	dBc/Hz	At divider output Δf=3MHz, BW=1Hz, PLL in lock
VCO gain	Kvco		700		MHz/V	
PLL						
Main divider divide ratio	N_{DIV}		229		-	
Reference divider divide ratio	R_{DIV}		4		-	
Phase comparator comparison frequency	fcomp		6.864		MHz	
Phase comparator DC gain	PHI		5		uA/cycle	
TCXO / X'tal input & CLKout output						
Input frequency	f_{OSC}		27.456		MHz	
Minimum input level	V_{IN}	500			mVpp	
CLKout output level	V_{OUT}	0.5			Vpp	RL/CL=50kΩ/15pF
	Duty	42		58	%	

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■ FUNCTIONAL DESCRIPTION

■ Operation / Testing mode setting

It is possible to set the state of the input pins MODE, ClkEN and ChipEN to select the operating mode and set a test mode for testing purpose.

Table 1. Test mode setting and its operating mode

MODE			Status of the RFIC
No.	ClkEN	ChipEN	
1	L	L	**Sleep mode**: all circuitry powered down, CLKout is “H”, IM,IS are “L”
2	L	H	**Operation mode**: activate circuits in nominal operation
3	H	L	**Standby mode**: Only OSC input buffer and CLKOUT output buffer are activated to provide a system clock to other Ics, IM,IS are “L”
4	H	H	**Operation mode**: activate all circuits in nominal operation

■ Setting of the Loop band of the Phase locked loop

The PLL uses an external loop filter. An on-chip resistor defines its charge pump output current. This allows the loop filter to be designed to obtain the best loop bandwidth of the closed loop for generating a good local signal for the down conversion system.

Design parameters:

Parameter	Symbol	Value	Unit
Phase comparator DC gain	PHI	5	uA/cycle
Oscillator gain	Kvco	700	MHz/V
Oscillator frequency	fvco	3143.712	MHz
Reference frequency	Fref	27.456	MHz
Reference divider ratio	Nref	4	

Calculated example for PLL bandwidth of 25kHz:

Name	Value	Unit
C1	77	pF
R2	22	kOhm
C2	1.16	nF

(See the application sheet notes for actual values on chipset)

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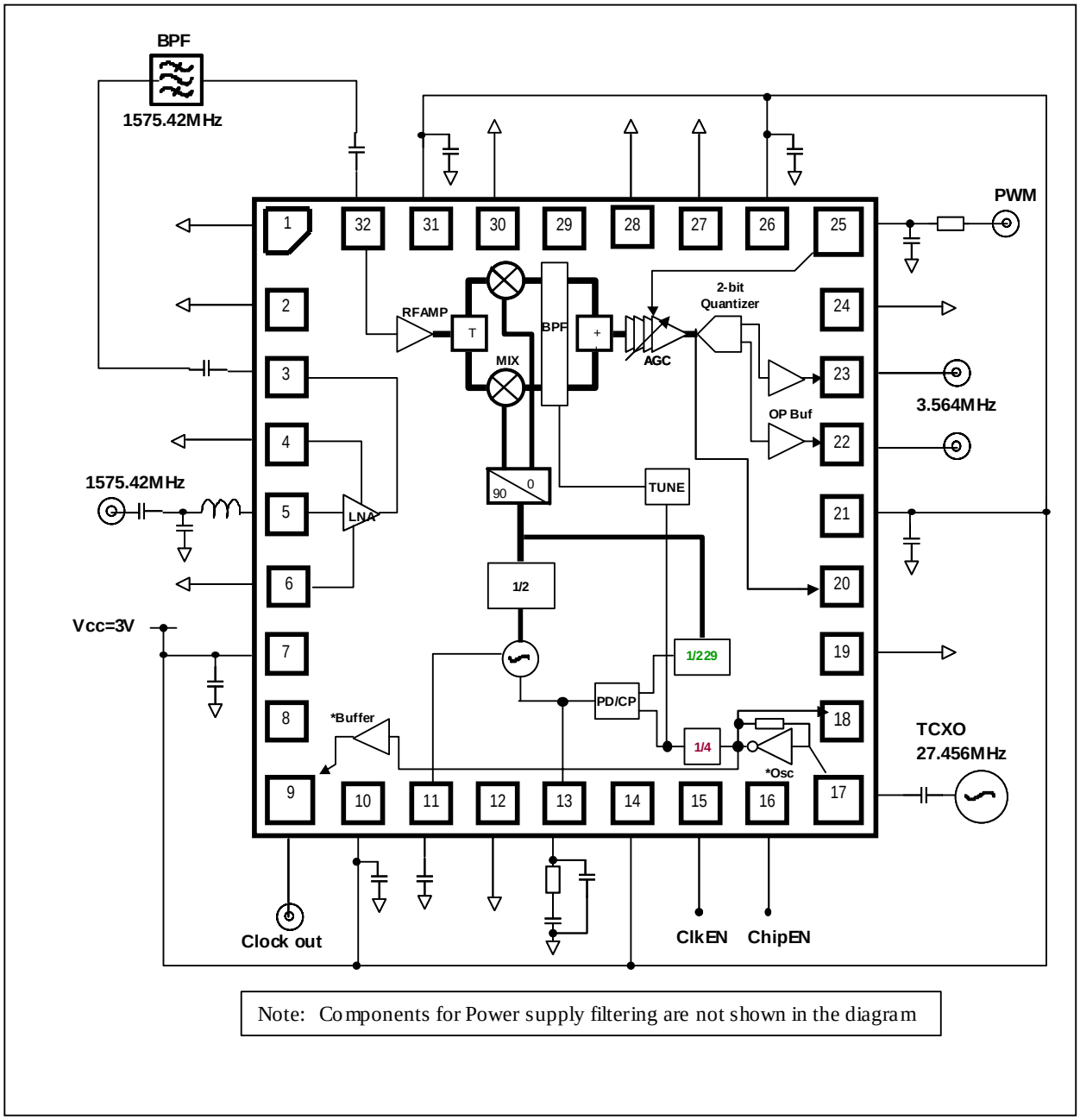
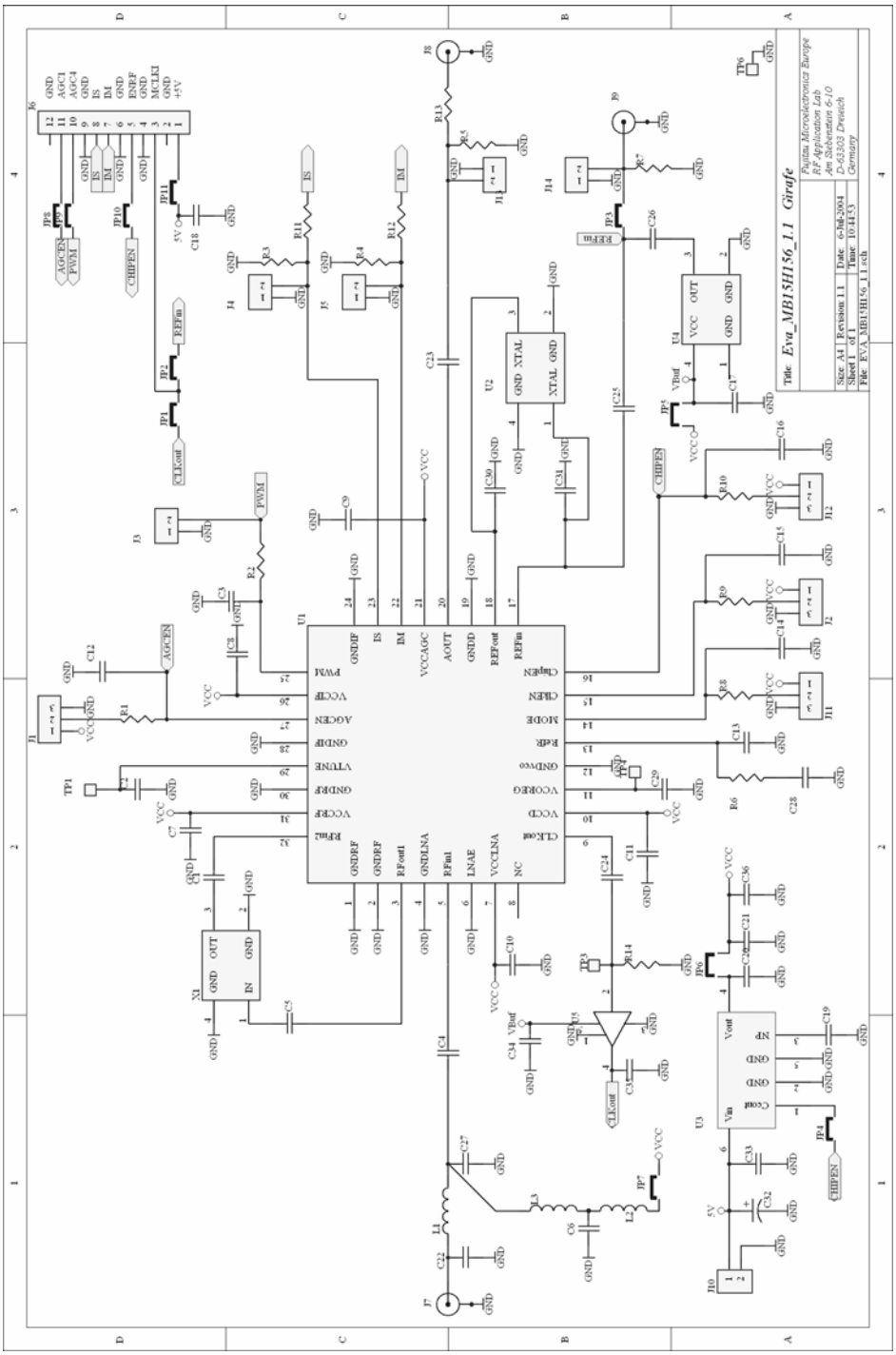
- **APPLICATION EXAMPLE**



Note: A correct power-up sequence of RF front-end and digital baseband is ensured by proper dimensioning of the coupling capacitors, see the system application sheet.

■ EVALUATION BOARD DIAGRAM

EPR1015B EVA Board V1.0 Prelude One “EVA_ePR1015B 1.1” (4 Layer)



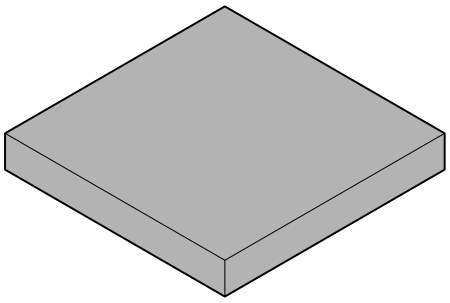
Component Values ePR1015B Evaluation Board V1.1

Designator	Value	Footprint	Comment
C1	1n	0603_C	
C2	1n	0603_C	
C3	100n	0603_C	
C4	1n	0603_C	
C5	1n	0603_C	
C6	1n	0603_C	
C7	1nF	0603_C	
C8	10nF	0603_C	
C9	10nF	0603_C	
C10	10nF	0603_C	
C11	10nF	0603_C	
C12	100p	0603_C	
C13	100p	0603_C	
C14	100p	0603_C	
C15	Nc	0603_C	
C16	Nc	0603_C	
C17	100p	0603_C	
C18	100n	0603_C	
C19	100n	0603_C	
C20	100n	0603_C	
C21	100n	0603_C	
C22	Nc	0603_C	
C23	10n	0603_C	
C24	Nc	0603_C	
C25	47p	0603_C	
C26	10n	0603_C	
C27	nc	0603_C	
C28	1n	0603_C	
C29	100nF	0603_C	
C30	33pF	0603_C	
C31	nc	0603_C	
C32	10µF	3528	
C33	100nF	0603_C	
C34	1n	0603_C	
C35	Nc	0603_C	
C36	1u	0805	
R1	10k	0603_R	
R2	10R	0603_R	
R3	nc	0603_R	
R4	nc	0603_R	
R5	15k	0603_R	
R6	nc	0603_R	
R7	51R	0603_R	
R8	47k	0603_R	
R9	47k	0603_R	
R10	47k	0603_R	
R11	0R	0603_R	
R12	0R	0603_R	
R13	0R	0603_R	Nc
R14	nc	0603_R	Nc
L1	3n3	603	Nc
L2	100n	603	
L3	100n	603	
J1	CONN3	SW_JUMP	
J10	DC-Power	POWER2	
J11	MIX	SW_JUMP	
J12	LNA	SW_JUMP	
J13	CONN2	BRIDGE1	
J2	CONN3	SW_JUMP	
J3	CONN2	BRIDGE1	
J4	CONN2	BRIDGE1	
J5	CONN2	BRIDGE1	
J6	CHEETAH_HEADER	FCC_ZIF12	
J7	SMA	SMA_END_LAUNCH	
J8	SMA	SMA_END_LAUNCH	
J9	SMA	SMA_END_LAUNCH	
JP1	JUMP_SOLD	Solderbridge	
JP2	JUMP_SOLD	Solderbridge	Nc
JP3	JUMP_SOLD	Solderbridge	
JP4	JUMP_SOLD	Solderbridge	Nc
JP5	JUMP_KLEIN	BRIDGE1	
JP6	JUMP_KLEIN	BRIDGE1	
JP7	JUMP_SOLD	Solderbridge	VCC for active antenna
JP8	JUMP_SOLD	Solderbridge	Nc
JP9	JUMP_SOLD	Solderbridge	Nc
JP10	JUMP_SOLD	Solderbridge	
JP11	JUMP_SOLD	Solderbridge	Nc
TP1	TP	SIP1	Nc
TP3	TP	SIP1	Nc
TP4	TP	SIP1	Nc
TP6	TP	SIP1	Nc
U1	EPR1015B	BCC32-2	
U2	XTAL_SMD	XTAL_SMD3.2x2.5	nc
U3	TK11230CMI	SOT-23L6	nc
U4	TCXO	XTAL_SMD3.2X2.5, 27.456MHz	
U5	74LVC1G125	SOT-23_5	nc
X1	FAR-F6EA-1G5754-L2AZ	F6EA 2 x 1.6 mm	Fujitsu
Nc= cot connected			

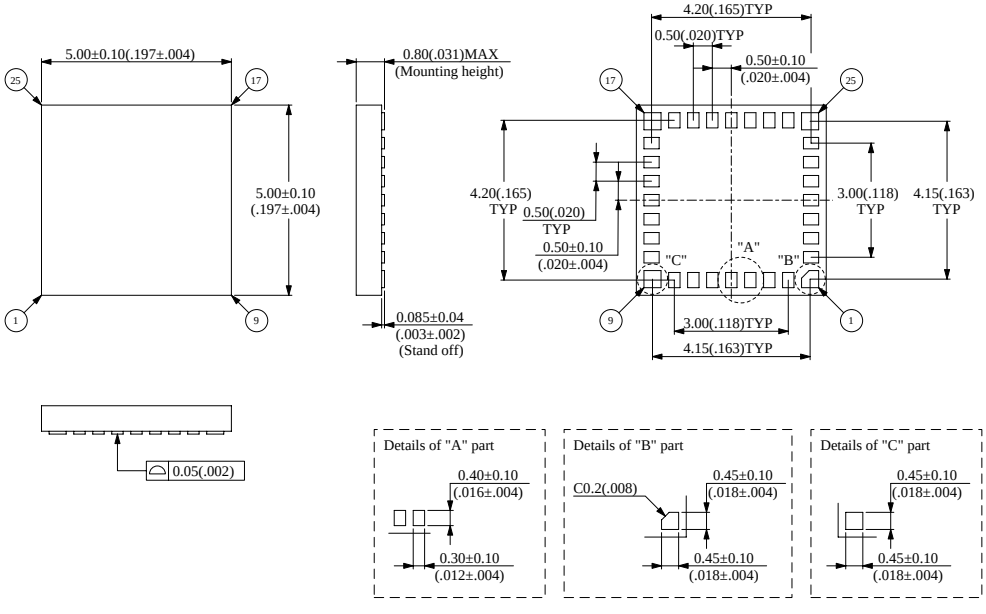
PACKAGE DIMENSIONS

(BCC-32)

LCC-32P-M08

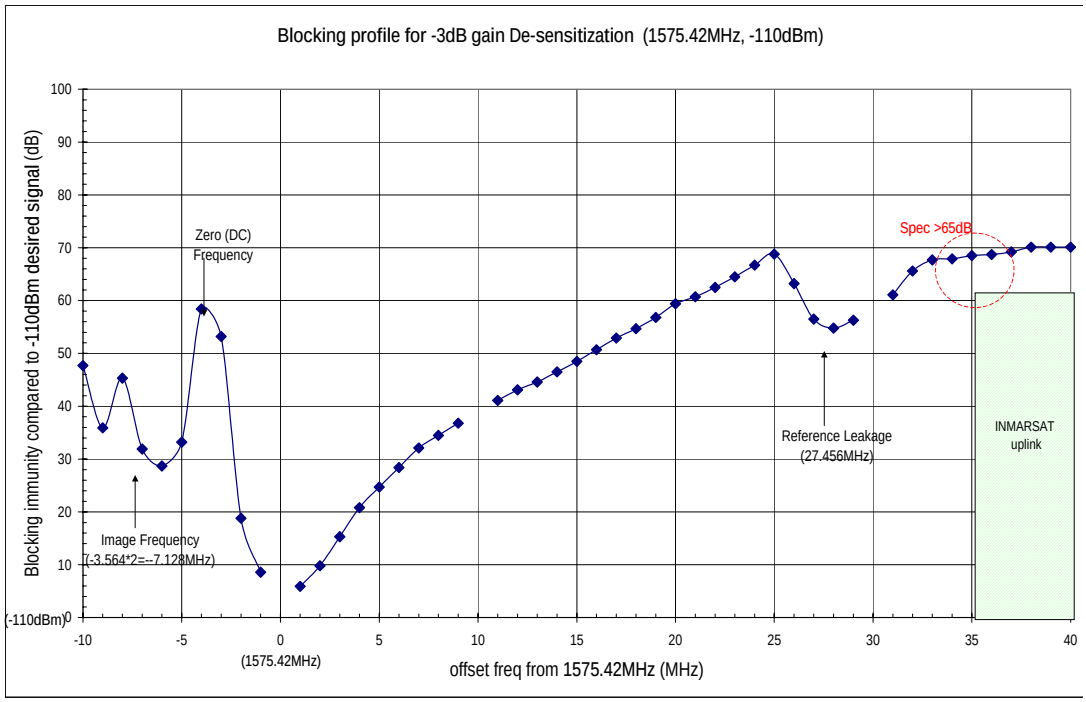


(LCC-32P-M08)

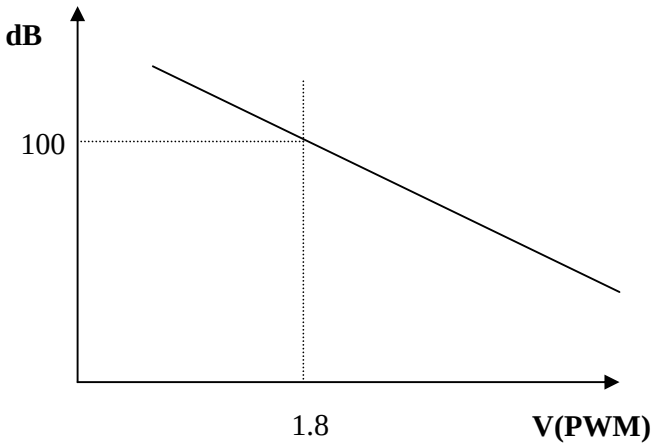


Appendix

A: Blocking profile. Note: A blocker is not stronger than –75dBm at the LNA input



B: Overall gain vs. control voltage at PWM pin (characteristic only)



This target specification is the design specification for product development. After more examination is done, this target may change

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