Product Datasheet
eOP1100B

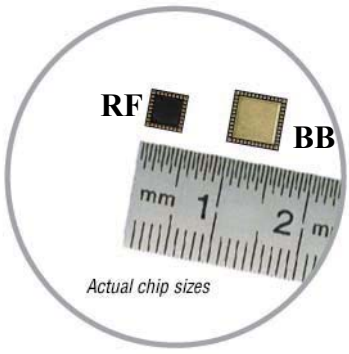
Opus One

GPS / A-GPS Receiver Baseband Processor

August 2006
Version 1.4
Opus One Datasheet

The eRide Opus One (eOP1100B) is a GPS/A-GPS receiver baseband processor with novel decoding algorithms achieving 44,000 effective correlators. It is capable of working indoors and decoding low sensitivity signals down to -157.5 dBm during acquisition and tracking. Opus One takes in a single low-IF input from a GPS-RF frontend chip and supplies location measurement data to the host processor. A serial UART interface allows for easy interfacing to modems on mobile handsets and other host applications.

The chip is fabricated using 0.11 um CMOS technology with 1.2V supply, offering low power consumption and small package size. The Opus One baseband processor, together with its Prelude One RF front-end chip make up eRide's low cost, high performance GPS/A-GPS solution.



Package Dimensions
7 mm x 7 mm

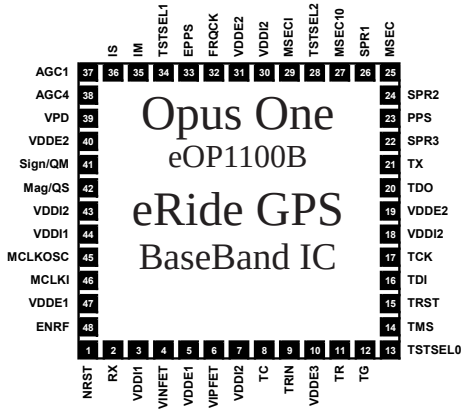
Features:

- Supports GPS L1-band, C/A code
- High indoor sensitivity of –157.5 dBm achieved utilising 44,000 effective correlators (both acquisition & tracking)
- Works in both Autonomous mode and Assisted-GPS mode
- Fast TTFF of typically 3s when hot and <40s from cold
- Typical power dissipation when tracking is 15 mW and 69 mW during acquisition.
- Accuracy of 7m outdoors (CEP 95%) and <20m indoors
- Small 7x7mm foot-print using 48-pin BCC++ package
- Host interface via a simple serial port
- Control software requires only 4 MIPS and runs as a background process on the host CPU.
- 1 Hz or 2.5 Hz update rate
- 3V (I/O) and 1.2V (core) supply voltage
- Industrial operating temperature of -40^{O}C to +85^{O}C
- Small BOM (low component count, size and cost)

Target Applications

- Multi-carrier, Multi-standard cellular handsets
  W-CDMA, GSM/EDGE, UMTS, PDC, CDMA, etc.
- Telematics, Automotive/Navigation/Security and Gaming/Tracking

PIN ASSIGNMENT



Note : Top View

Contents List

1 GPS/A-GPS Chipset

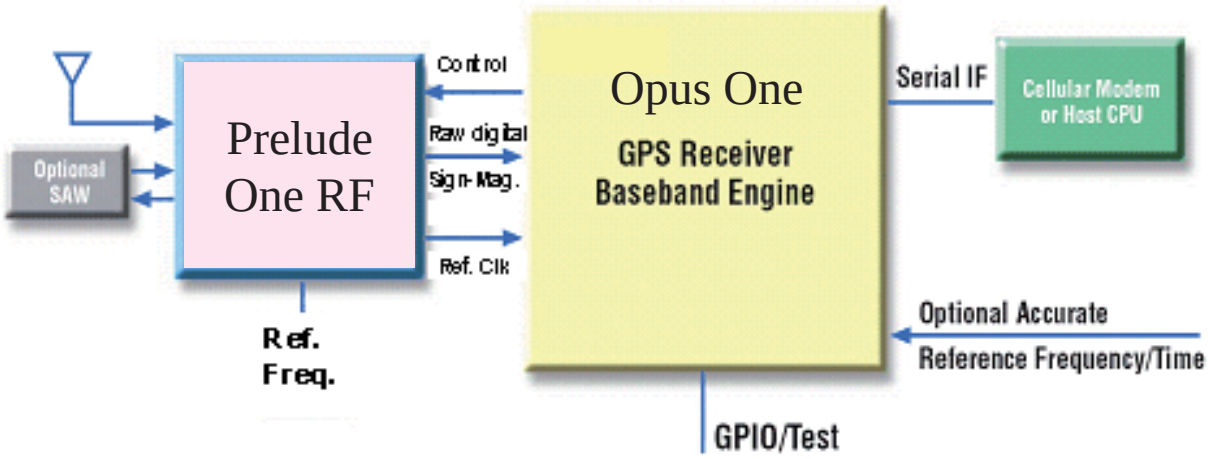


Figure 1 Complete System Block Diagram

Figure 1 shows a block diagram of eRide's high performance GPS/A-GPS (both autonomous and assisted modes) receiver solution. Two eRide devices, the Prelude One RF chip and the Opus One Baseband Processor, are offered. Opus One includes a hardwired engine with 44,000 effective correlators, and the RF chip integrates all the required analogue functions. The reference frequency is supplied from an external TCXO that is further compensated by a proprietary software based algorithm. An RF SAW filter may be required in applications where very high level blocking signals must be tolerated. This solution is capable of working indoors and receiving/decoding low sensitivity signals down to -157.5 dBm during acquisition and tracking. It also can operate completely autonomously or in assisted mode.

The Baseband Processor takes in a single input of the raw digital navigation data from the RF chip and, after processing, communicates the fix measurements data to the host processor via a simple serial UART interface. The control software runs on a host CPU and requires around 4-MIPS. This software runs as a background process that does not interfere with key tasks on the host processor and requires no real time interrupts.

This Baseband Processor chip is fabricated using 0.11 μm CMOS technology with 1.2V internal power supply resulting in low current consumption.

In environments where temperature changes are slow, the complete system may use an AT-cut crystal oscillator to generate the reference frequency. In this case, an oscillator circuit integrated on the eRide RF chip may be used. Patented compensation algorithms help to stabilise the frequency and relax the requirements on the crystal.

Typical System Features include:

- Supports GPS L-band C/A code .
- High indoor sensitivity down to -157.5 dBm for both acquisition and tracking.
- Works in both assisted GPS mode and also autonomous mode.
- Fast TTFF typically 3s when hot and <40s from cold (outdoors). Aided light-Indoor TTFF 5-8 secs
- Typical system (using the Opus One Baseband chip plus the ePR1015B BiCMOS RF chip together in a demonstration board) satellite tracking power dissipation is 86mW. Typical system power dissipation is 124 mW when acquiring satellites (using 2.7V/1.2V supplies).
- Accuracy of 7m outdoors (CEP 95%) and <20m indoors.
- Update rate of 1 Hz (also can integrate for 2.5 secs when indoors).
- Typical leakage current in deep sleep mode is <100uA (25^{O}C).
- Complete BOM components foot-print of ~85 mm^2 (eOP1100B 7x7mm 48-pin BCC package, RF chip 5x5mm 32-pin BCC package).
- Opus One to host interface is via a simple serial UART port. The host can be a phone platform or any simple MCU.
- Control software runs on a host CPU as a background process, and does not need High MIPS or large RAM.
- Supply voltages are 3V (2.7-3.6V) for I/O pins and 1.2V (1.1-1.3V) for the core logic.
- All chips handle Industrial operating temperature range (-40 deg C to +85 deg C).
- The RF chip (ePR1015B) has the GPS Front end Tuners with on-chip IF-Filters, VCO, Osc & LNA.
- Small BOM in terms of total components size, count and cost.

2 Functional Description

Opus One is a high performance GPS/A-GPS Receiver Baseband Processor. A functional block diagram of this chip is shown in Figure 2.

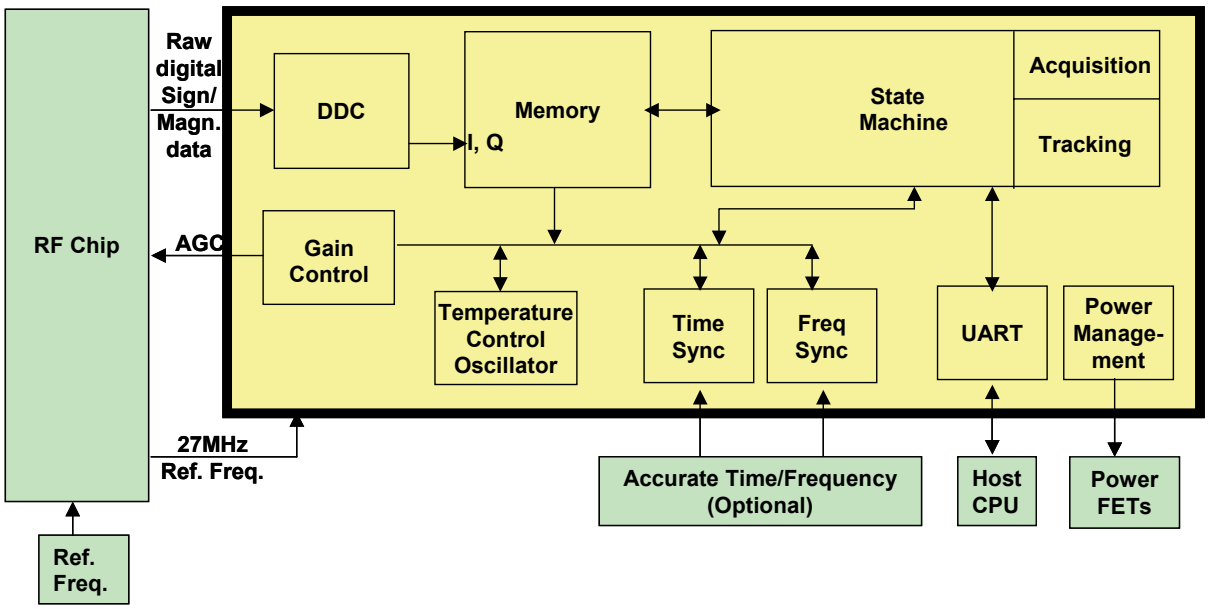


Figure 2 Opus One Functional Block Diagram

2.1 Reference Frequency

Opus One implements a patented "software compensated crystal oscillator" algorithm that helps it to tolerate crystal or other reference frequency instability.

A reference frequency clock is supplied from the RF chip and input to Opus One. This is required to be 27.456 MHz with +/-2 ppm accuracy (all causes), and <0.016 ppm/s stability (drift + microjumps).

The eRide GPS/A-GPS chipset requires a dedicated 27.456 MHz. Using a dedicated Crystal/TCXO makes this system independent of the application environment around it and allows operation either autonomously or in assisted mode with a modem.

2.2 Host CPU and Control Software

To ease interfacing of Opus One to any CPU / host product, a serial port (UART) interface is implemented.

The UART interface is configured to 57600 bps, in 8-bit format with odd parity and 1-stop-bit.

The Control software is written in C and is OS independent. Figure shows the structure of the control software residing on the host CPU.

The software is run as a background process on the Host and requires no real-time interrupts, no host libraries and no RTOS. The processing power required will be dependent on the application and whether GPS-aiding

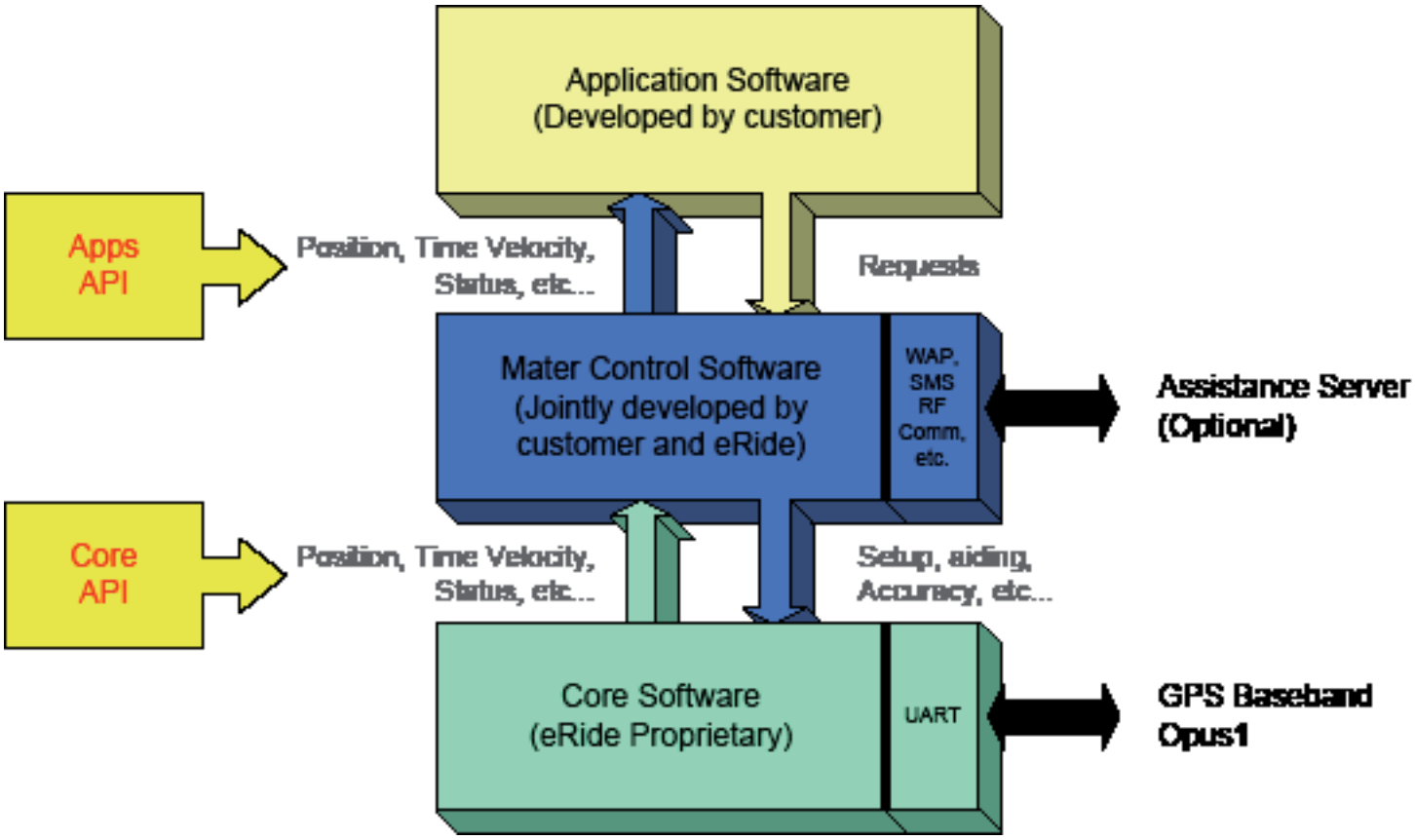


Figure 3 Control Software Layers

is required; normally some 4-6 MIPS will be required from Host CPU.

The code footprint varies dependent on the application and efficiency of the application code. For example, an autonomous only implementation on an ARM7TDMI platform resulted in the overall software footprint requiring around 198KB ROM and 70KB RAM on the Host CPU.

Two levels of API libraries are available to the customer. The first layer has a "Core API" library that includes functions to perform the basic control decisions for the receiver run mode including setup, aiding availability/type and required minimum accuracy for measurements, see section 2.2.1.

Customers will tailor the control code based on their requirements, together with eRide's application engineers. eRide can supply appropriate wire/wireless interface adapters (WAP, RFcomm, TCP/IP, etc.) as well as appropriate aiding-data protocol (3GPP, IS801, NMEA0183 etc.) for communicating with the aiding server hosted by the operator. This layer will also contain and maintain OS specific functions that shall include the standard communication protocols via ports including the UART and TCPIP/WAP/etc.

The second layer of API library will be supplied to customers to assist development of end-user applications such as mapping, directions, boundary areas and security alarms. It also supports/ manages basic location measurement requests for data such as position, velocity, time and gps status.

Details of the Control software and API libraries are described in a separate document, but an introduction is included in section 2.2.1.

Porting the Control Software to any customer specific platform is eased by having the whole code in the C programming language. eRide will assist with porting and/or optimising this Control software to any customers CPU.

Opus One takes its reference frequency and the raw IF sign/magnitude data from the RF chip, performs the GPS processing and sends the measurements to the host CPU, where the control software will provide the final PVT (position, velocity, and time) results.

2.2.1 Core API Introduction

The API library reside on the host CPU/MCU and controls Opus One. The library consists of three input functions and one output function. The input functions are called by the sample application. The output function is called by the master and must be implemented by the same application. These are:

Input Functions

int erStartClient()

This function is called to start the client. It will create a thread and return immediately.

int erStopClient()

This function is called to stop the client. It will not return until all client threads have completed, resources

have been freed and Opus One is in a shutdown state.

int erSetAidingOptions(erAidingStruct aiding)

This function is called to configure the GPS aiding to be used. It must be called before the call to erStartClient(). If erStartClient() is not preceded with a call to this function, the client will run in autonomous mode.

Output Function

int erProvidePvt(erPvtStruct erPvt)

The Master will call this function when it has PVT data available. This function is expected to return immediately. The argument is a structure containing the PVT data and is defined below.

An example application code is shown in Section .7

Resulted Measurements available are:

Table 1: Example of the measurements available from Opus One

GPS time of this report
Time of position fix
Bitmasked flag detailing the type of fix calculated
Number of SVs in fix
Indicates source of chosen solution
If chosenfix is subsolution, indicates SV that removed to calculate fix
Indicates source of reported altitude
ECEF position coordinates in meters
LLA position coordinates in radians, radians, meters
Filtered ECEF position coordinates in meters
Filtered LLA position coordinates in radians, radians, meters
ECEF velocity coordinates in meters per second
ENU velocity coordinates in meters per second
Filtered ECEF velocity coordinates in meters per second
Filtered ENU velocity coordinates in meters per second
Filtered clock bias in meters
Filtered clock drift in meters per second
PDOP of fix
Accuracy of filtered position in meter
Accuracy of filtered velocity in meters per second
Accuracy of filtered bias in meter
Accuracy of filtered drift in meters per second
Horizontal accuracy of filtered position in meter per second
Vertical accuracy of filtered position in meter per second
Horizontal speed in meter per second
Vertical speed in meter per second
Direction of user movement in radians

2.3 Core Engine State Machines

The heart of the Opus One is the GPS IP from eRide Inc. This IP includes a GPS processing engine and the Control software on the host processor (see section).

To achieve a fix, the algorithms on the processing engine employs two different state machines, the Opus State Machine (OSM) and Firmware State Machine (FSM):

1. Opus State Machine (OSM)

The OSM manages all the code-delays, frequency-offset, correlation as well as interfacing between the hardware and all peripherals.

2. Firmware State Machine (FSM)

The FSM offers 3 modes of operation:

1. An Indoor State Machine (IDSM) with a high sensitivity acquisition and tracking block capable of searching and tracking to a sensitivity of –155 dBm (using 1 sec integration time) and -157.5 dBm (with 2.5 sec integration time).
2. An Outdoor State Machine (ODSM) which searches all 32 satellites, with –145 dBm sensitivity without intervention from the Host CPU.
3. A Time-Tracking State Machine (TSM) which collects navigational data and provides synchronous measurements so that GPS time and navigation data can be decoded and utilized without Host CPU interrupts.

This GPS processing engine has 44000 effective correlators available to either search 32 satellites at several time/frequency hypotheses, or search thousands of time/frequency hypotheses for a few satellites that are in view. Search windows (time/frequency hypotheses) are flexible by design and configurable for each satellite.

3 Performance

3.1 Usage modes

The following sections detail the target functionality and performance.

The Opus One receiver can be set up to perform in two possible modes:

3.1.1. Autonomous mode

In this mode, Opus One will decode Navigation data from Satellites only. It therefore needs a good signal strength (to as low as -145 dBm) while decoding for first fix. TTFF in this mode is slowest as Opus One downloads the ephemeris data at 50 bps (taking ~30 secs). Once Opus One has received ephemeris and Almanac data (i.e. become hot), then it can go on to supply fix measurements indoors with sensitivity down to -157.5 dBm. An application/user may supply some time or location assistance, if available (e.g. handset time or cell location currently in use), resulting in improved TTFF.

3.1.2. Assisted mode

Either on wake-up from autonomous mode, or upon a request for a fix after current aiding data has expired (ephemeris is valid for 4 hours, and refreshed every two hours), Opus One shall request Navigation data from the aiding server via the implemented interface (SMS, WAP, TCP/IP, RRLP, etc.) using any aiding-data format (3GPP/2, IS801, OMA-SUPL, etc.). Opus One will continue to supply fixes and update its ephemeris/almanac as time permits and without further resource/help from the aiding server. Therefore assistance can be good for hours.

Assisted, MS-Based mode of operation achieves the fastest TTFF.

Opus One aiding interface is independent of the aiding server. eRide Inc. has a worldwide reference network and can supply the aiding server to any operator and/or infrastructure companies.

3.2 Sensitivity

The algorithm implemented in Opus One can acquire and track weak signals down to -155 dBm using 1 sec integration time and -157.5 dBm while integrating for 2.5 sec. Opus One achieves this sensitivity in both autonomous and assisted modes as well as during both acquisition and tracking of satellites.

3.3 Time To First Fix

The TTFF (Time To First Fix) is as follows:

- Hot[1] or aided start outdoors take typically 3 seconds.
- From Cold[2] on autonomous start, outdoors, takes typically less than 40 seconds.
- Warm[3] start takes about 5-30 seconds, outdoors.

*1 Hot start means that the receiver has full Ephemeris navigation data, Almanac, time to within 10 sec, and knows its location to within 150 Km. (similar to being aided)

*2 Cold start means the receiver has no knowledge of RTC, its location, Almanac or Ephemeris and no aiding is available.

*3 Warm start means the receiver has any combination of time, current location, Almanac, and Ephemeris.

Figure 4 shows result from a run with a GPS simulator for various satellites sensitivities and the corresponding receiver performance. For this, the fix rate achieved was 100% with 1 Hz updates (1 second integration) and the accuracy is 50% CEP. Aiding used was: Time known to within 10 secs; location within 150 km; ephemeris/almanac given; and TCXO (2.0 ppm).

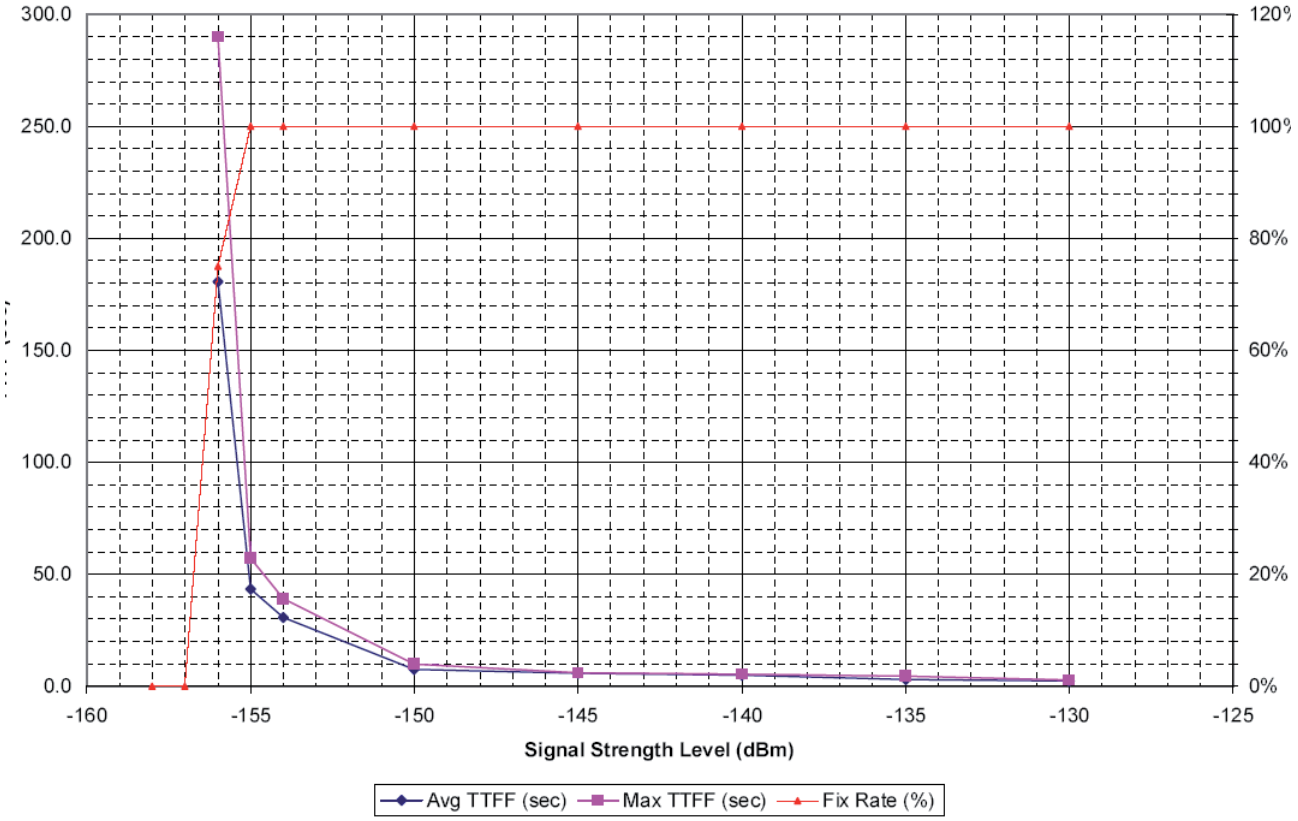


Figure 4: TTFF degradation with increased Sensitivity

3.4 Accuracy

Opus One's GPS/A-GPS engine meets the requirements for FCC-E911 regulations for October 2005.

The results from Opus One performance shows that it is possible to achieve <20m accuracy indoors and in urban canyons. This kind of accuracy was previously only available in open spaces outdoors.

Figure 5 below shows the accuracy performance of Opus One (1 Hz updates)

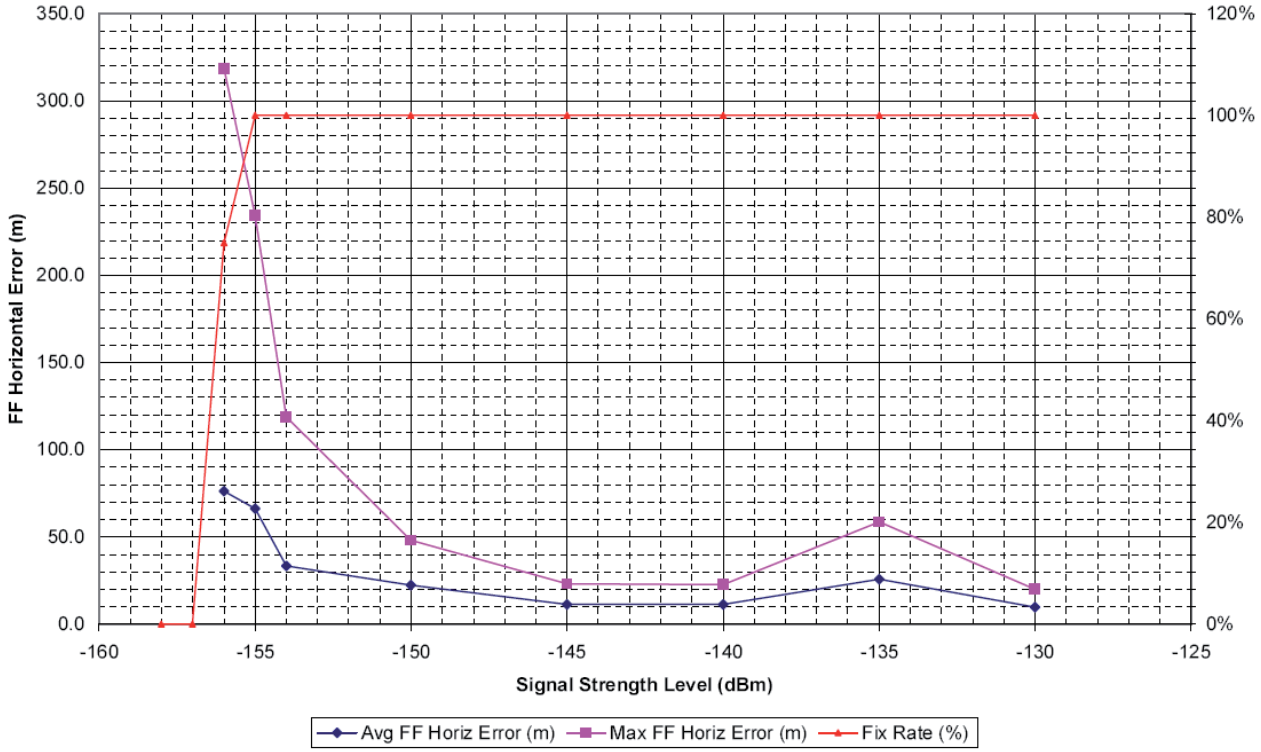


Figure 5: Accuracy degradation with increased Sensitivity

3.5 Power Consumption & Power Modes

All power saving modes are controllable by the customer via the control software. Opus One's Power saving modes are detailed below.

3.5.1 Deep Sleep Mode

The deep sleep mode has the lowest power consumption. Use of separate on-chip supply regions allows full power down of most of the chip and stopping of all clocks. Power to the PowerSW region (see Figure 9) together with its related I/O signals is OFF, and MCLK (the master clock for all internal clocks) is turned OFF as well. Signal ENRF is OFF and signal NRST is in a disabled state. Wake-up from deep sleep is invoked by a low transition on the RX pin, which then puts the chip into the RTC mode.

3.5.2 Real Time Clock (RTC) Mode

In RTC mode the majority of the logic is not clocked, but power supply is ON for the entire chip (both power regions of Figure are powered up). ENRF is OFF and only Millisecond (MSECxx) outputs and peripherals are turned ON with clocks running. All other clocks are turned OFF to save dynamic power.

3.5.3 Search Mode

In this mode the search is performed, which means highest power dissipation. All the clocks are running, multiple satellites are being searched, and the ENRF is ON.

3.5.4 Track Mode

In Track mode, a certain number of satellites are tracked with fine adjustments in code search. Not all clocks are running, so power dissipation is lower than search mode. ENRF is ON.

4 Package and Pins Functionality

This section describes Opus One's package and pins.

4.1 BCC48++ Package

A mechanical drawing of the BCC++ package used for Opus One is illustrated in Figure 6. Critical dimensions are:

- Lead pitch: 0.50 mm
- Package width x package length: 7.00 mm x 7.00 mm
- Sealing method: Plastic mold
- Mounting height: 0.80 mm (max)

As can be seen in Figure 6, a 5.1 x 5.1 mm metal pad exists on the bottom-side of the package. This is wired internally to the die *Vss* pads. The metal pad must be connected to ground with multiple pads/vias, since there are no *Vss* pins around the periphery of the package.

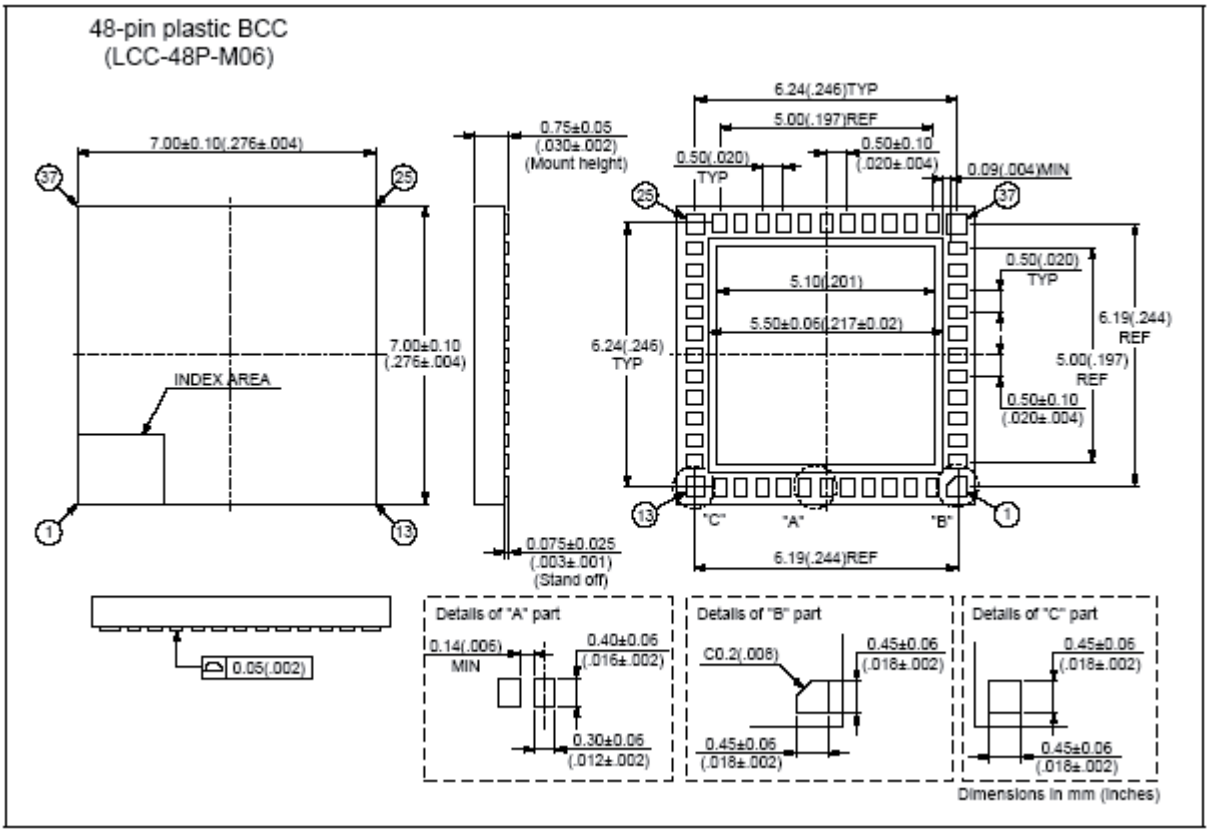


Figure 6: Diagram of the BCC48++ package

4.2 Complete pin list and buffer/region types

Pin	Pin Name	Pin Function	Type	Func	I/O Buffer Type	PU/PD	deep sleep	Voltage Domain	Jtag ring
1	NRST	Power-on RESET	I	I	IOBSI3TNSMNNXXX1		ON	VDDI1/VDDE1	NO
2	RX	UART receive pin	I	I	IOBSI3TNNMNNXXX1		ON	VDDI1/VDDE1	NO
3	VDDI1	1.2V Supply for region 1	P	I					
4	VINFET	Gate control for P-FET	B	O	IOBSB3TNNMNNTNL1		ON	VDDI1/VDDE1	NO
5	VDDE1	3V Supply for region 1	P	I					
6	VIPFET	Gate control for N-FET	B	O	IOBSB3TNNMNNTNL1		ON	VDDI1/VDDE1	NO
7	VDDI2	1.2V Supply for region 2	P	I					
8	TC	TCO capacitor connect	B	O	IOBXXTLBF3N50MN0		OFF	VDDI2/VDDE3	NO
9	TR_IN	XTAL input pin	I	I	IOBXXTLIF3NNNNN0		OFF	VDDI2/VDDE3	NO
10	VDDE3	3V Supply for region 3	P	I					
11	TR	TCO thermistor connect	B	O	IOBXXTLBF3N50MN0		OFF	VDDI2/VDDE3	NO
12	TG	TCO Gate	I	I	IOBXXTLIF3NNNNN0		OFF	VDDI2/VDDE3	NO
13	TSTSEL0	Test select0	I	I	IOBSI3TNNMDDXXX1	PD	OFF	VDDI2/VDDE2	YES
14	TMS	JTAG TMS	I	I	IOBSI3TNNMUDXXX1	PU	OFF	VDDI2/VDDE2	
15	TRST	JTAG TRST	I	I	IOBSI3TNNMUDXXX1	PU	OFF	VDDI2/VDDE2	
16	TDI	JTAG TDI	I	I	IOBSI3TNNMUDXXX1	PU	OFF	VDDI2/VDDE2	
17	TCK	JTAG TCK	I	I	IOBSI3TNNMNNXXX1		OFF	VDDI2/VDDE2	
18	VDDI2	1.2V Supply for region 2	P	I					
19	VDDE2	3V Supply for region 2	P	I					
20	TDO	JTAG TDO	O	O	IOBSO3TNXXXXTNL1		OFF	VDDI2/VDDE2	
21	TX	UART TRANSMIT	O	O	IOBSO3TNXXXXTNL1		OFF	VDDI2/VDDE2	YES
22	SPR3	Spare Test Pin3	B	I	IOBSB3TNNMDDTNL1		OFF	VDDI2/VDDE2	YES
23	PPS	Pulse Per Second	B	O	IOBSB3TNNMNNTNL1		OFF	VDDI2/VDDE2	YES
24	SPR2	Spare Test Pin2	I	I	IOBSI3TNNMDDXXX1		OFF	VDDI2/VDDE2	YES
25	MSEC	1 msec output	B	O	IOBSB3TNNMNNTNL1		OFF	VDDI2/VDDE2	YES
26	SPR1	Spare Test Pin1	B	I	IOBSB3TNNMDDTNL1		OFF	VDDI2/VDDE2	YES
27	MSEC10	10 msec output	B	O	IOBSB3TNNMNNTNL1		OFF	VDDI2/VDDE2	YES
28	TSTSEL2	Test select2	I	I	IOBSI3TNNMDDXXX1	PD	OFF	VDDI2/VDDE2	YES
29	MSECI	Msec Interrupt	B	O	IOBSB3TNNMNNTNL1		OFF	VDDI2/VDDE2	YES
30	VDDI2	1.2V Supply for region 2	P	I					
31	VDDE2	3V Supply for region 2	P	I					
32	FRQCK	Freq Differentiator clock	I	I	IOBSI3TNSMDDXXX1	PD	OFF	VDDI2/VDDE2	YES
33	EPPS	External Pulse/second	I	I	IOBSI3TNNMDDXXX1	PD	OFF	VDDI2/VDDE2	YES

Table 2: Opus One functional and supply pin list

Table 2: Opus One functional and supply pin list

34	TSTSEL1	Test select1	I	I	IOBSI3TNNMDDXXX1	PD	OFF	VDDI2/VDDE2	YES
35	IM	Imag. Magn. of I/Q input	I	I	IOBSI3TNNMNNXXX1		OFF	VDDI2/VDDE2	YES
36	IS	Imag. Sign of I/Q input	I	I	IOBSI3TNNMNNXXX1		OFF	VDDI2/VDDE2	YES
37	AGC1	AGC control	B	O	IOBSB3TNNMNNTNL1		OFF	VDDI2/VDDE2	YES
38	AGC4	AGC control	O	O	IOBSO3TNXXXXTNL1		OFF	VDDI2/VDDE2	YES
39	VPD	DC TEST VPD	I	I	IOBSVPDF3NNN1		OFF	VDDI2/VDDE2	
40	VDDE2	3V Supply for region 2	P	I					
41	Sign/QM	IF Sign data, or Real Magn. of I/Q input	I	I	IOBSI3TNNMNNXXX1		OFF	VDDI2/VDDE2	YES
42	Mag/QS	IF Magn. data, or Real Sign of I/Q input	I	I	IOBSI3TNNMNNXXX1		OFF	VDDI2/VDDE2	YES
43	VDDI2	1.2V Supply for region 2	P	I					
44	VDDI1	1.2V Supply for region 1	P	I					
45	MClkOsc	XTAL oscillation cell out	B	I	IOBXXTLBF3R50MN0		ON	VDDI1/VDDE1	NO
46	MCLKI	master 27.456Mhz clock	I	I	IOBXXTLIF3NNNNN0		ON	VDDI1/VDDE1	NO
47	VDDE1	3V Supply for region 1	P	I					
48	ENRF	Enable RF	B	O	IOBSB3TNNMNNTNL1		ON	VDDI1/VDDE1	NO

Figure 7 also shows a top view of the Opus One package with pin names.

Buffer Cell Types

Buffer Cell	**Type**
IOBSB3TNNMDDTNL1	3.3V-I/F Bidirectional True buffer, Normal, 33Kohm-PullDown, L_type
IOBSB3TNNMNNTNL1	3.3V-I/F Bidirectional True buffer, Normal, L_type
IOBSI3TNNMDDXXX1	3.3V-I/F Input True buffer, Normal, 33Kohm-PullDown
IOBSI3TNNMNNXXX1	3.3V-I/F Input True buffer, Normal
IOBSI3TNNMUDXXX1	3.3V-I/F Input True buffer, Normal, 33Kohm-Pullup
IOBSI3TNSMDDXXX1	3.3V-I/F Input True buffer, TTL-Schmitt, 33Kohm-PullDown
IOBSI3TNSMNNXXX1	3.3V-I/F Input True buffer, TTL-Schmitt
IOBSO3TNXXXXTNL1	3.3V-I/F Output True buffer, Normal, 3-state, L_type
IOBSVPDF3NNN1	3.3V-I/F Static current control
The following are Oscillator cells (R = with feedback):	
IOBXXTLBF3N50MN0	Bidirectional buffer for Oscillator with Enable (3.3V CMOS, Schmitt Input)
IOBXXTLBF3R50MN0	Bidirectional Oscillator buffer with Enable and 1Mohm feedback (3.3V CMOS, Schmitt Input)
IOBXXTLIF3NNNNN0	Input buffer for Oscillator (3.3V CMOS)

Abbreviations:

Columns 4 and 5: I=input, O=Output, and B=Bidirectional P=Power.

Column 7: PD=Pull down, and PU=Pull Up.

Column 8: shows if a signal is ON or OFF during sleep-mode.

Column 10: shows if the pin is included in the Jtag Chain or not.

4.3 Pin Assignment

There are 5 functional groups of pins described in this section. A top view of Opus One's pins is illustrated in Figure . Note that this package has a ground pad on the belly centre of the package and normally is referred to as pin 49.

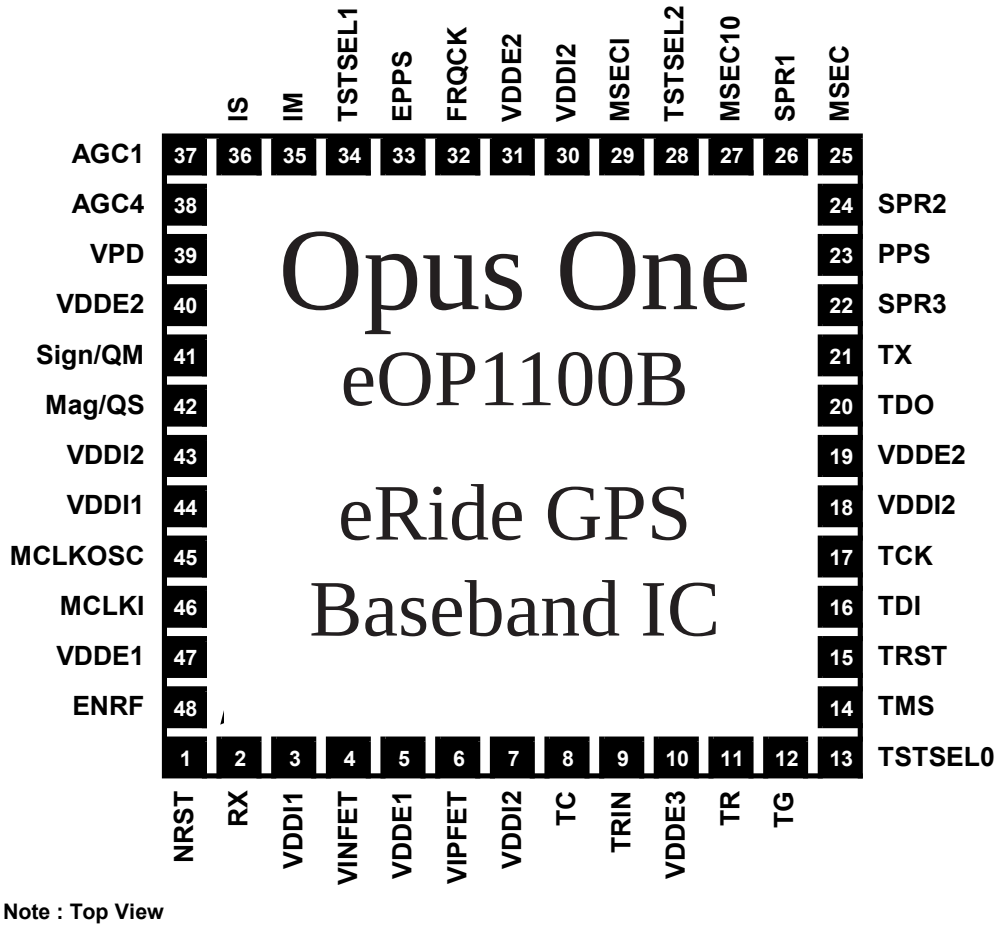


Figure 7: Top view of Opus One (eOP1100B) Pins

4.3.1 Supply Voltage pins

All VSS pads (not shown in Figure 7 because VSS has no external pin on the sides of the package) are connected to the ground pad frame as supplied by the BCC++ package.

Table 3: Voltage supply pins

Pin No.	Pin Name	Description
3,44	VDDI1	VDD Internal 1.2V supply for powerON region
5, 47	VDDE1	VDD External 3.0V supply for powerON region
7, 18, 30, 43	VDDI2	VDD Internal 1.2V supply for powerSW region
19, 31, 40	VDDE2	VDD External 3.0V supply for powerSW region
10	VDDE3	VDD External 3.0V supply for Oscillator cells

4.3.2 MOSFET Switch pins

Table 4: Power FET pins

Pin No.	Pin Name	Input/ Output	Description
6	VIPFET	O	gate control of the N-type FET power switch for Core voltage supply. This signal switch the 1.2V supply to all the VDDI2 pins located in powerSW region of Figure 9. See Figure 14 for circuit. VIPFET=0 in Sleep Mode and VIPFET=1 in RTC/Active modes
4	VINFET	O	gate control of the P-type FET power switch for I/O voltage supply. This signal switch the 3.3V supply to the VDDE2 and VDDE3 pins in powerSW region of Figure 9. See Figure 14 for circuit. VINFET=1 in Sleep Mode and VINFET=0 in RTC/Active modes

4.3.3 Host CPU - eOP1100B UART interface Pins

Table 5: UART Interface pins

Pin No.	Pin Name	Input/ Output	Description
2	RX	I	UART interface: Receive signal from the Host CPU
21	TX	O	UART interface: Transmit signal to the Host CPU

The UART interface protocol is controlled by the Control software residing on the host processor. It is asynchronous and is fixed at Baud rate 57600 bps, in 8-bit format with odd parity and 1-stop-bit.

4.3.4 Additional Functional pins

Table 6: TCO, PPS and Accurate Reference pins

Pin No.	Pin Name	Input/ Output	Description
23	PPS	O	Pulse per second output
33	EPPS	I	External pulse per second. used for accurate reference time if available. The control software will initiate sync of this signal with the receivers RTC
32	FRQCK	I	Accurate reference frequency input pin. This signal is used to connect an existing accurate reference source if available. The control software will initiate sync of this signal with the reference frequency
8	TC	O	TCO Capacitor port. See Figure 8
11	TR	O	TCO Thermistor port. See Figure 8
12	TG	I	TCO Gate port. See Figure 8
9	TR_IN	I	TCO external short with pin TR. See Figure 8

4.3.5 Opus One - Prelude One interface Pins

The signals below interface between eOP1100B and the RF chip. They are all asynchronous

Table 7: RF chip interface pins

Pin No.	Pin Name	Input/ Output	Description
41	Sign/QM	I	**IF Sign data input, or Real-part of Magnitude data for I/Q input** **Sampled by eOP1100B on both edges of 27.456 MHz clock** **0=negative signal, 1=positive**
42	Mag/QS	I	**IF Magnitude data input, or Real-part of Sign data for I/Q input** **Sampled by eOP1100B on both edges of 27.456 MHz clock** **0=below threshold, 1= above threshold**
36	IS	I	Imaginary-part of Sign data for I/Q input, else pull low for IF input
35	IM	I	Imaginary-part of Magnitude data for I/Q input, else pull low for IF input
46	MCLKI	I	27.456 MHz reference system clock. High when inactive
48	ENRF	O	enable/disable of the RF chip. 0=disable, 1=enable (active)
37	AGC1	O	Used for control of AGC in RF chip. If the RF chip has the ability to either control its own gain or be externally controlled, AGC1 can be used to enable/disable this internal control. 0='internal mode' 1=external mode'
38	AGC4	O	For control of an RF chip AGC in 'external mode', AGC4 is a PWM output with selectable sign. Linear in dB change between 0V (max gain) and 2V (min gain), and flat gain beyond 2V

4.3.6 JTAG and Test pins

Table 8: Test pins

Pin No.	Pin Name	Input/ Output	Description
16	TDI	I	JTAG test
20	TDO	O	JTAG test
17	TCK	I	JTAG test
15	TRST	I	JTAG test
14	TMS	I	JTAG test
39	VPD	I	eRide test pin
13	TSTSEL0	I	eRide test pin
34	TSTSEL1	I	eRide test pin
28	TSTSEL2	I	eRide test pin
26	SPR1	I	eRide test pin
24	SPR2	I	eRide test pin
25	MSEC	O	Test pin (1msec output)
27	MSEC10	O	Test pin (10msec output)
29	MSECI	O	Test pin (msec interrupt)

5 Electrical Characteristics

5.1 Maximum ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section 5.2. Also, exposure to the Absolute Maximum Conditions for extended periods may affect device reliability. Table 10 below shows the maximum ratings for the CS91 process:

Table 9: Maximum ratings (Vss=0V)

Parameter	Symbol	Requirements	Unit
Power supply voltage	VDD	-0.5 to 1.8 (*1) -0.5 to 4.0 (*2)	V
Input voltage	VI	-0.5 to VDD+0.5 (=1.8V) (*1) -0.5 to VDD+0.5 (=4.0V) (*2)	V
Output voltage	VO	-0.5 to VDD+0.5 (=1.8V) (*1) -0.5 to VDD+0.5 (=4.0V) (*2)	V
Storage temperature	TST	-55 to 125	^{o}C
Junction Temperature	Tj	-40 to 110	^{o}C
Ambient Temperature	Ta	-40 to 85	^{o}C

(*1) internal gate part (VDDI pins)
(*2) I/O part (VDDE pins)

5.2 Recommended Operating Conditions

Recommended operating conditions set values for normal device operation. As long as the device is used within the ranges, electrical characteristics (DC and AC characteristics) are guaranteed.

5.3 Power Supply Recommended Operating Conditions

Table 10: Dual power supply (VDDE=2.7-3.6V, VDDI=1.1-1.3V, VSS=0V)

Parameter		Symbol	Rating			Unit
			Minimum	Typical	Maximum	
Supply voltage		VDDE	2.7	3.0	3.6	V
		VDDI	1.1	1.2	1.3	V
H level input voltage	1.2V CMOS	VIH	VDDIx0.7	-	VDDI+0.3	V
	3.3V CMOS		2.0	-	VDDE+0.3	V
L level input voltage	1.2V CMOS	VIL	-0.3	-	VDDIx0.3	V
	3.3V CMOS		-0.3	-	0.8	V
Ambient Temperature		Ta	-40	-	85	^{o}C

5.4 DC characteristics (Dual power: VDDE=3.3V/VDDI=1.2V)

Measurement conditions: VDDE=2.7-3.6V, VDDI=1.1-1.3V, VSS=0V, Ta= -40 to 85 ^{o}C

Table 11: DC characteristics (Dual power: VDDE=3.3V/VDDI=1.2V)

Parameter	Sym-bol	Condition	Value			Unit
			Min.	Typ.	Max.	
Supply Current	IDDS		-	-	-	mA
H-level output voltage	VOH4	3.6V Output IOH=-100uA	VDDE-0.2	-	VDDE	V
	VOH2	1.2V Output IOH=-100uA	VDDI-0.2	-	VDDI	V
L-level output voltage	VOL4	3.3V Output IOL=100uA	0	-	0.2	V
	VOL2	1.2V Output IOL=100uA	0	-	0.2	V
H-level output V-I characteristics	-	VDDE=3.3±0.3V	see Figure 8 below			-
L-level output V-I characteristics	IOL	VDDE=3.3±0.3V	see Figure 8 below			-
Input leakage current	IL	(excluding pullup/down leakage)	-	-	±10	uA
Pull up/Pull down resistance	Rp	3.3V	15	33	70	kΩ
Power dissipation		Real Time Clock mode		2		mW
Power dissipation		Satellites tracking after a fix		15		mW
Power dissipation		High sensitivity (Indoors) searching/ Acquiring mode from cold		77		mW
Power dissipation		Six Satellites Outdoor and 2 satellites Indoor- from cold acquiring		69		mW
Power dissipation		Outdoor satellites searching- from hot		32		mW
Power dissipation		Deep Power down mode		<99		uW
Power dissipation		Wake Up from Deep Power down with		60		mW

5.5 CS91 Output Buffer V-I Characteristics

Conditions for the output buffers are shown Figure 8 (with conditions in Table 12) below:

Table 12: Output buffer V-I Characteristics

	Min (process slow)	Typ (process typical)	Max (process fast)
Ta (^{o}C)	85	25	-40

Table 12: Output buffer V-I Characteristics

	Min (process slow)	Typ (process typical)	Max (process fast)
VDD (V)	2.7	3.3	3.6

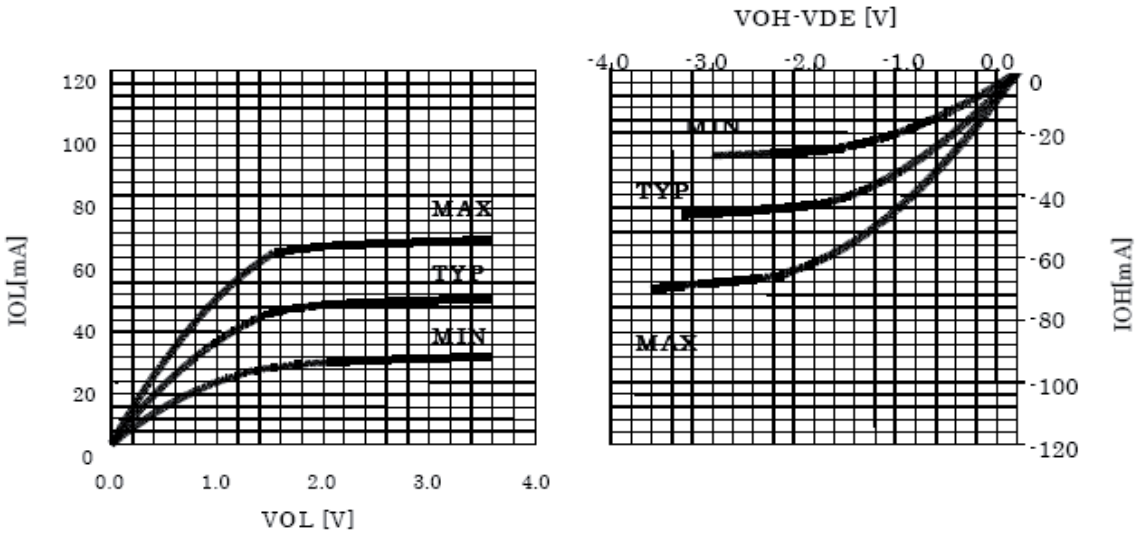


Figure 8 : 3.3V standard CMOS IO type V-I characteristics

5.6 Input/Output Pin Capacitance

Table 13 shows input/output pin capacitance.

Measurement conditions: Ta=25^{o}C, VDD=VI=0V, f=1MHz

Table 13: Input/Output pin capacitance

Parameter		Symbol	Requirements	Unit
Input pin	-	CIN	3*	pF
Output pin	type	COUT	3*	pF
I/O pin	type	CI/O	3*	pF

* Capacitance varies according to the package and the location of the pin.

5.7 Power Sequencing

This section describes how VDDI and VDDE should be sequenced.

5.7.1 Power Regions

eOP1100B has two power regions (PowerON and PowerSW) enabling the optional removal of power to PowerSW whilst keeping required logic alive in the PowerON region. This minimises the supply current when eOP1100B enters deep sleep mode. Two external FETs (in a single package) are used to switch these regions ON and OFF as required, controlled by the eOP1100B VIPFET and VINFET pins.

PowerON consists of VDDI1 (1.2V) and VDDE1 (3.0V) and will only be switched off during a full system power down.

PowerSW consists of VDDI2 (1.2V) and VDDE2/3 (3.0V) and can be powered up or down during device operation, but should only be ON if the permanent supply is ON.

Figure 9 clarifies the various power regions and signal-pin locations in eOP1100B (not to scale). Note that pin 49 represents the metal pad underneath the whole chip and should be connected to ground.

The following Table 14 shows the status of the power supplies in the various power regions.

Table 14: Voltage supply to power regions

Name	Power	Max Current [mA]	Control	Pin Numbers	Deep sleep mode	RTC/Active mode
VDDE1	3.3V	10	F/W, Separate	5, 47	ON	ON
VDDE2	3.3V	10	F/W, Separate	19, 31, 40	OFF	ON
VDDE3	3.3V			10	OFF	ON
VDDI1	1.2V	30	F/W, Separate	3, 44	ON	ON
VDDI2	1.2V	150	F/W, Separate	7, 18,30	OFF	ON
GND	0V		hardware	49		

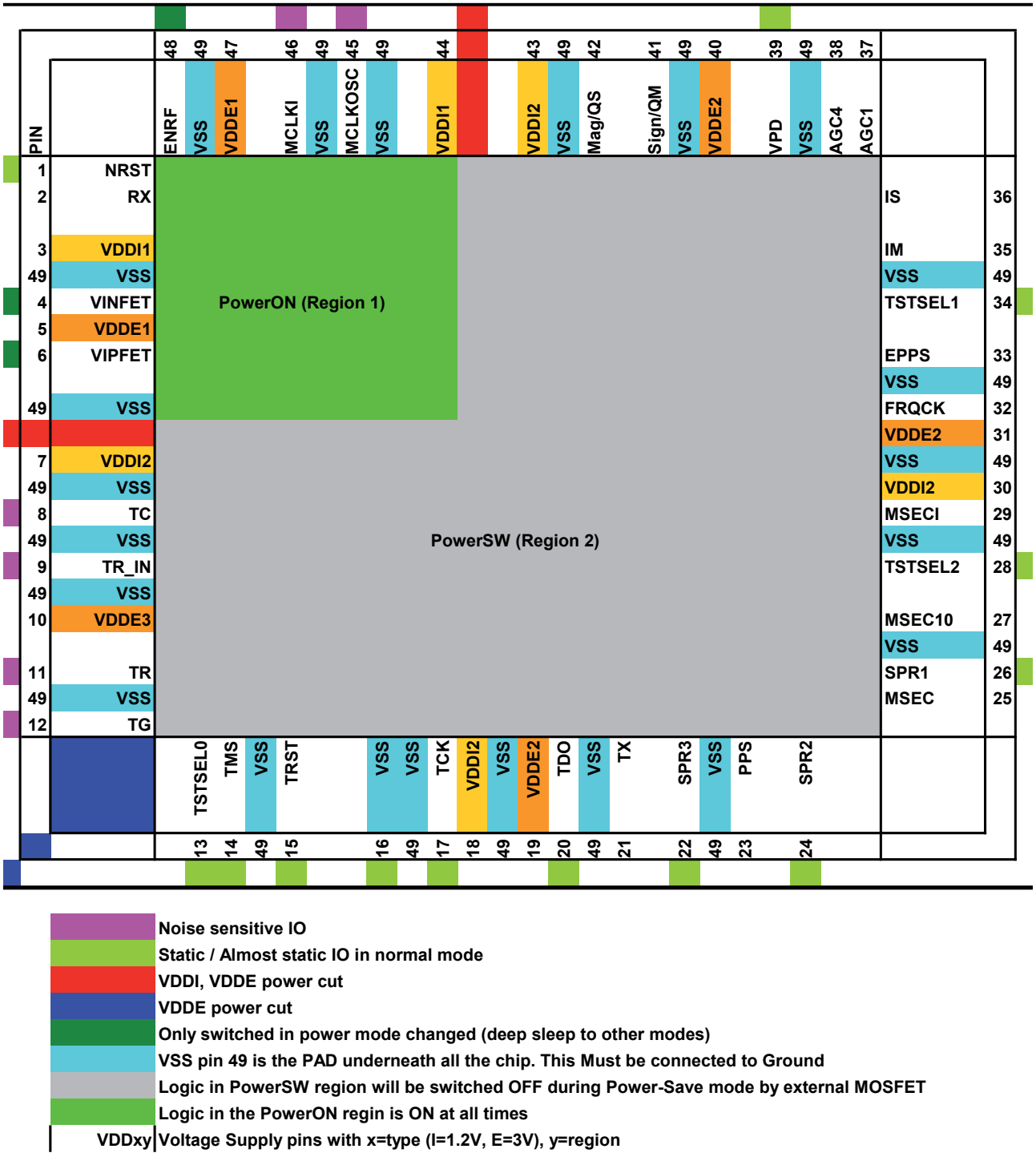


Figure 9: Top View of Opus One Baseband Power Supply Regions

5.7.2 Power on/off sequence

Note: To prevent reliability problems, VDDE should not be powered up whilst VDDI is off.

No external power switching:

If external power switching of the PowerSW region is not employed, power up of eOP1100B is relatively simple and the following power sequences are recommended.

Power-ON	V_{DDI} >>>>> V_{DDE} >>>>> Signal
Power-OFF	Signal >>>>> V_{DDE} >>>>> V_{DDI}

All V_{DDI} (1.2V) supplies should be enabled together and all V_{DDE} (3.0V) supplies should be enabled together.

NRST should be held low until all supplies are stable and MCLKI is receiving a clock (from the RF AFE). During power-up, the external clock signal fed to MCLKI should be stable (running with no glitches).

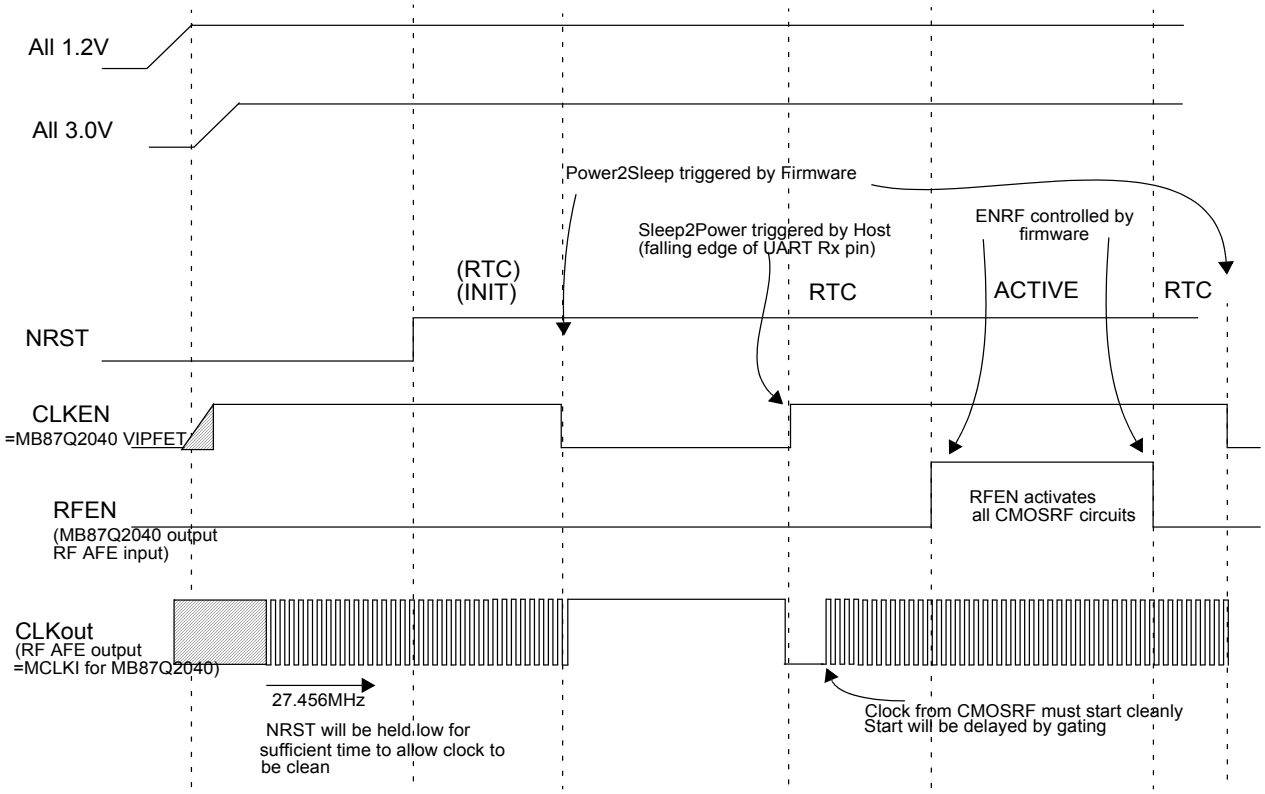


Figure 10 Power Sequences with no power switching

With external power switching:

If external power switching of the PowerSW region is employed, the power up sequence is more critical. The circuit shown in Figure 15 employs power switching which conforms to the sequencing recommendations illustrated in Figure 12.

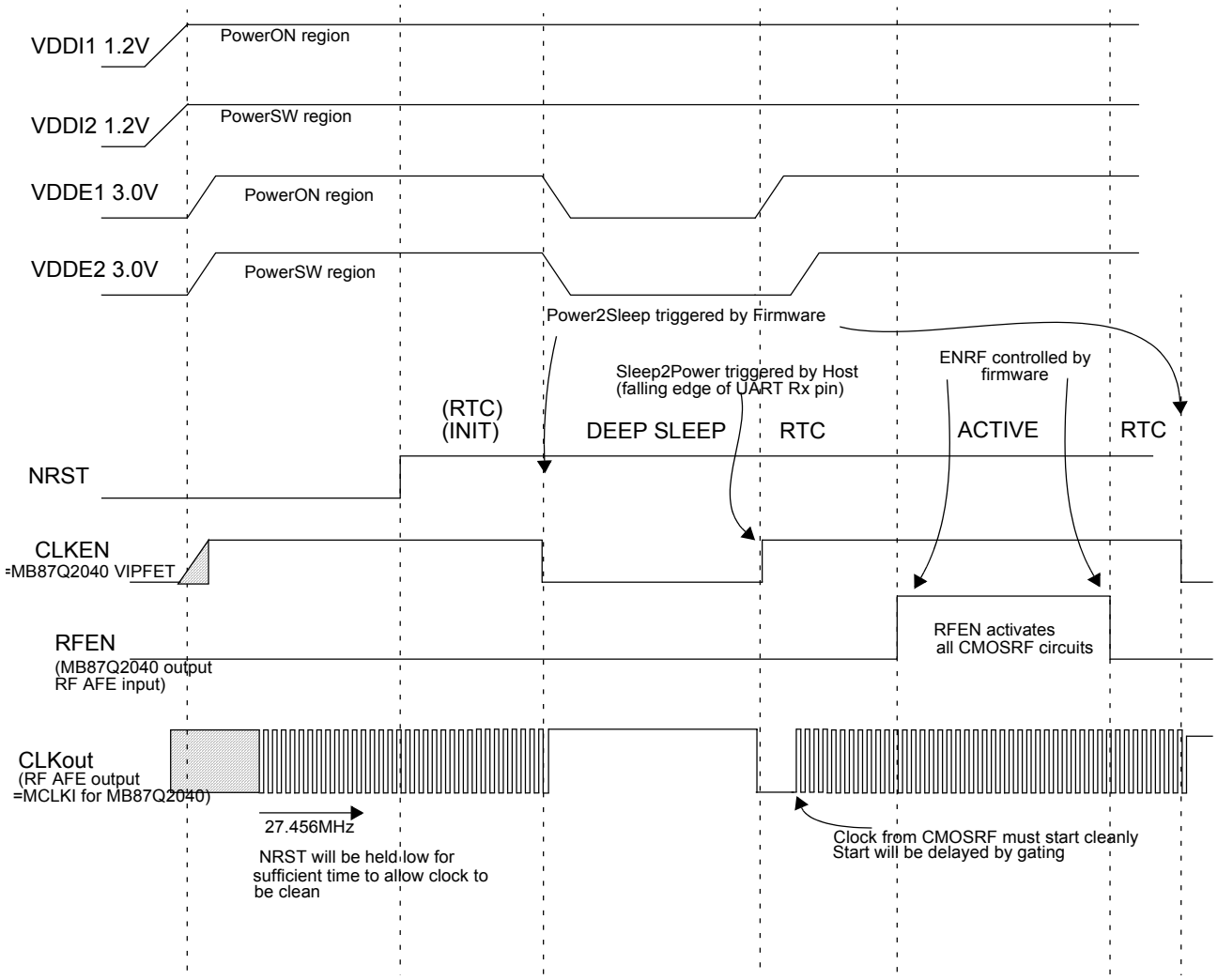


Figure 11 Power Sequences for power switching

Power-down sequence (deep sleep):

The power down is initiated from eOP1100B which sets VINFET=1 and VIPFET=0 shutting down the external switched supplies (VDDE2/VDDE3 and VDDI2) if power switching is employed.

VIPFET is wired to the CLKEN of the Prelude One RF, thus disabling the clock into MCLKI. Also all internal signal passing between eOP1100B's power regions are shut down.

Wakeup:

Before this sequence is started, all signals in the powerSW region are unknown and VDDI2 & VDDE2/VDDE3 are off if power switching is used. The following events occur at wakeup.

1. A falling edge on RX will trigger the wakeup sequence, then VIPFET and VINFET will change state and this shall power-up VDDI2 and VDDE2/3.
2. Once the supply is settled, NRST should be held low for at least 10ns after VDDI2/VDDE2 is stable.
3. During power-up the external clock signal fed to MCLKI should be stable (running with no glitches).

5.8 Boundary SCAN Design

When on Normal operation power (powerON and PowerSW are ON), set value "0" for more than 10ns to the TRST pin before starting the JTAG scan system operation, and the Boundary SCAN registers enter the system test mode.

6 Application Notes: Self contained Module

Figure 12 is a schematic diagram of component placement for a self-contained GPS/AGPS module.

This design has been built into an Evaluation board using 4-layers board (2-layers for all components, a ground layer and a power layer) for demo purposes. The resulted board size is 13 x 18 mm. A picture of this board is shown in Figure 13. The actual Evaluation Kit (EVK), including the USB interface board, is shown in Figure 12. A compact module can be arranged so to minimise noise and produce compact layout. The main devices used in the EVM, with sizes, are:

- Opus One (eOP1100B) is 7x7 mm
- Prelude One (ePR1015B) is 5x5 mm
- The Crystal is 3.2 x 2.5 mm (The EVM uses a 2.0 ppm TCXO device. This may not be required if other reference frequency is available within the host design, such as in a mobile handset)
- FET Switches are 2x2.1 mm and 1.7 x 1.7 mm (The FET are used to switch voltage supply to eOP1100B OFF/ON, so to reduce leakage current when the receiver is in sleep mode. The switched Vdd could also be used to power the RF chip ON/OFF. These FET's may not be needed if the host application some other power management scheme)
- SAW is optional dependent on application. (e.g. Fujitsu's FAR-F6EA-1G5754-L2AZ)
- Thermistor with 22 KOhm at 25oC (e.g. NTCCM20123FH222KC)
- Rest of components are capacitors, resistors, and an inductor.

NOTE: Before designing your board, please contact your eRide regional sales office (Americas, Europe or Asia) for the latest version of the schematics, BOM, layout recommendations and various approved parts used in this reference design board.

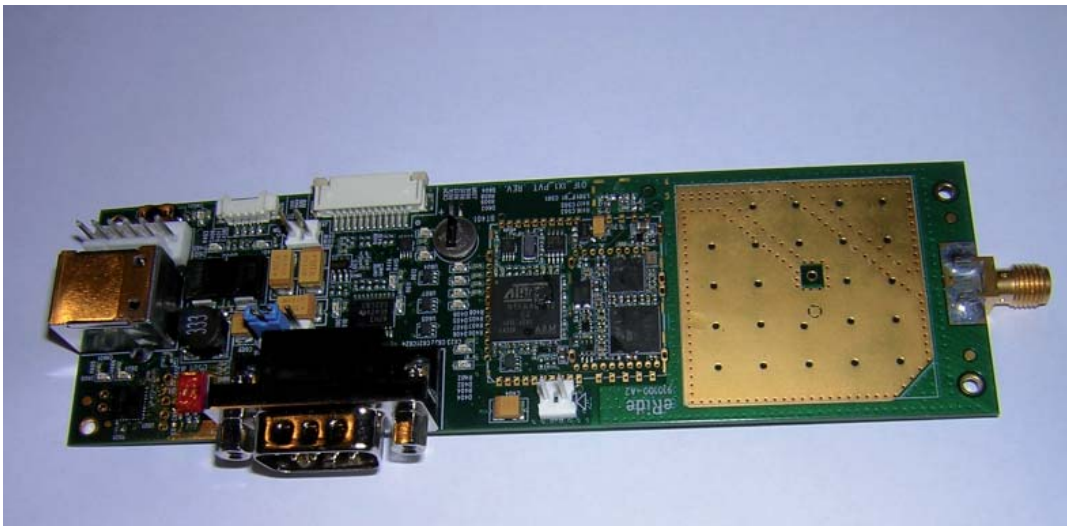


Figure 12: Photo of the EVK Demo Kit

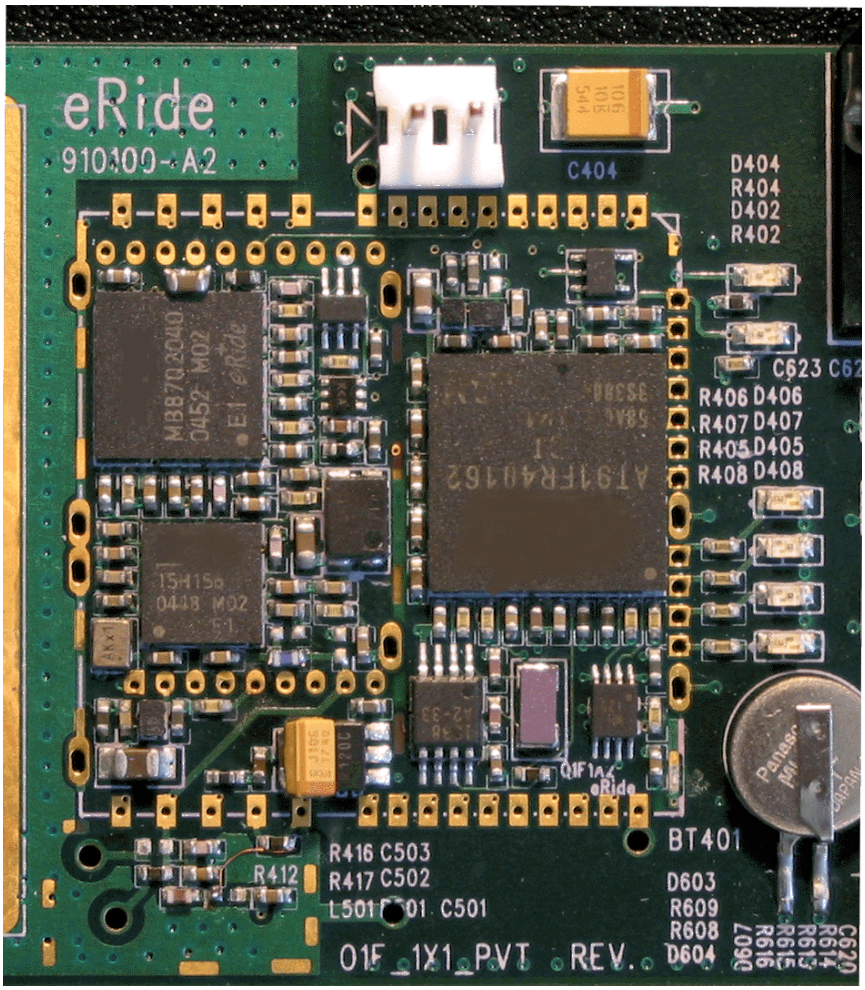
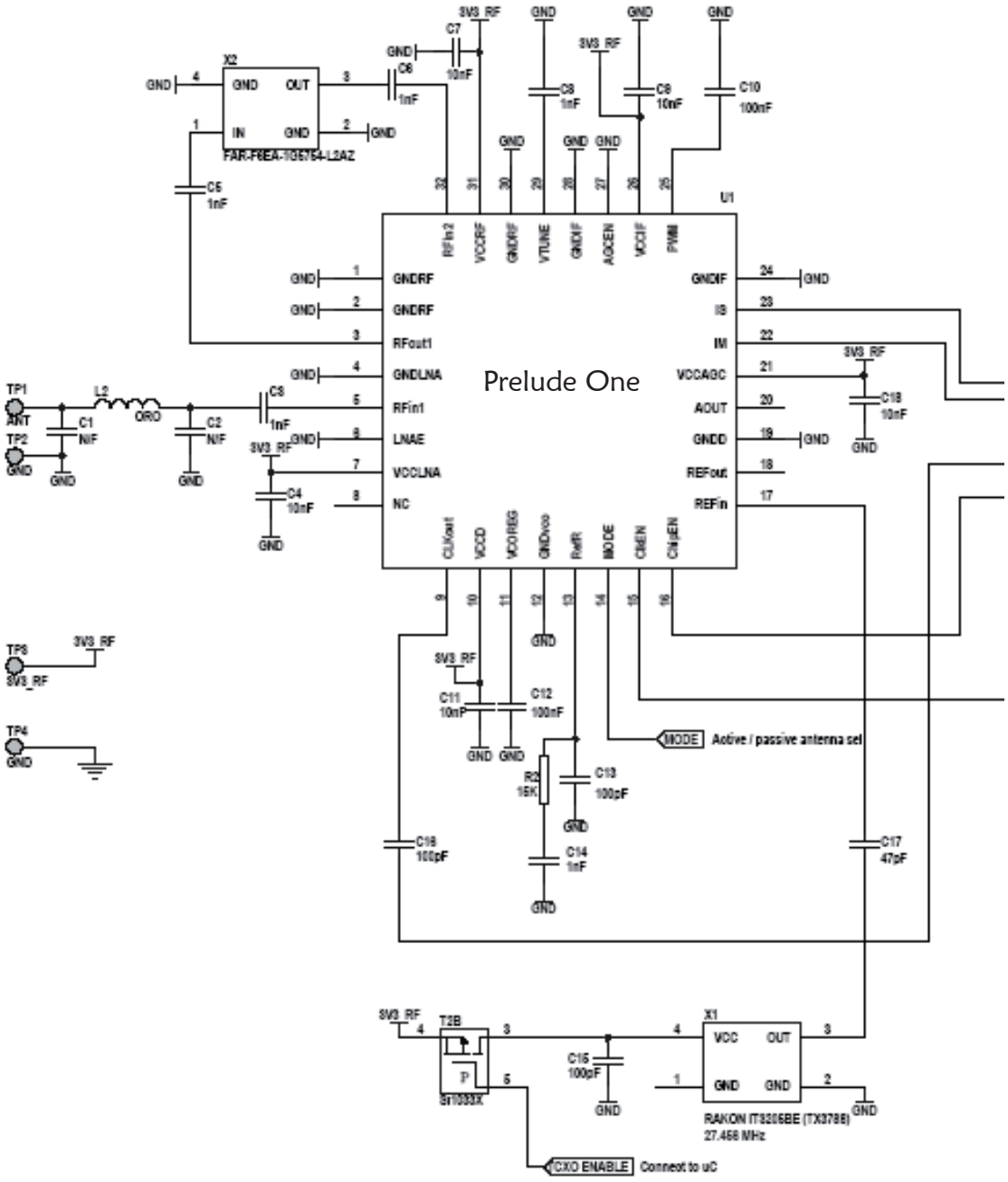
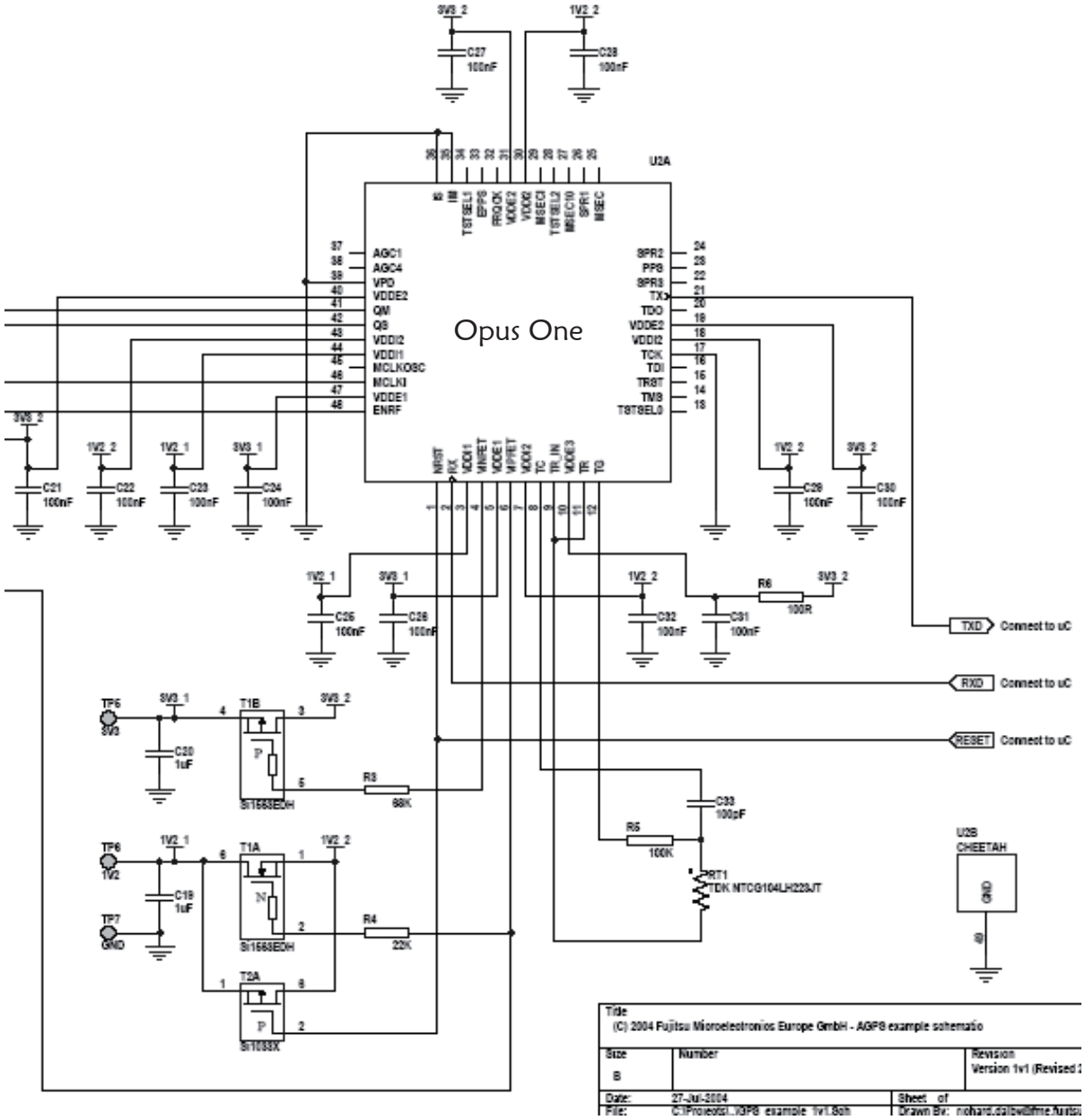


Figure 13: Photo of the Evaluation Kit single sided assembly board

Figure 13 show the complete active area to provide a GPS Position, Velocity and timing solution that provides NMEA output. The reference design, housed in a compact 25.4 x 25.4 mm (1 square inch) includes the eRide hardware measurement platform (Opus One + Prelude One) in a 13 x 18 mm layout area and the additional microprocessor host (in the remaining area). In hosted applications, the Opus One chipset leverage available resource available on the customer's board, therefore reducing the footprint of the GPS solution to a minimum (the Opus One chipset, SAW filter, TCXO and a few discrete matching components).





6 Application Notes: Application Example of API Code

The API library reside on the host CPU/MCU and controls eOP1100B The library consists of three input functions and one output function. The input functions are called by the sample application. The output function is called by the master and must be implemented by the same application. These are:

Input Functions

int erStartClient()

This function is called to start the client. It will create a thread and return immediately.

int erStopClient()

This function is called to stop the client. It will not return until all client threads have completed, resources have been freed and Opus One is in a shutdown state.

int erSetAidingOptions(erAidingStruct aiding)

This function is called to configure the GPS aiding to be used. It must be called before the call to erStartClient(). If erStartClient() is not preceded with a call to this function, the client will run in autonomous mode.

Output Function

int erProvidePvt(erPvtStruct erPvt)

The Master will call this function when it has PVT data available. This function is expected to return immediately. The argument is a structure containing the PVT data and is defined below.

An example application code is shown in Section 7.

Structure Definitions are:

```
     typedef struct {
     U32  pvtGpsTime;// GPS time of this report.
     U32  pvtFixTime;// Time of position fix.
     U8   pvtFixType;// Bitmasked flag detailing the type of fix calculated.
     U32  pvtFixSVs;// Number of SVs in fix.
     U8   pvtFixSource;// Indicates source of chosen solution.
     U8   pvtSubsolnSv;// If chosenfix is subsolution, indicates SV that removed
to calculate fix.
     U8   pvtAltSource;// Indicates source of reported altitude.
     S32  pvtPos[3];// ECEF position coordinates in meters.
     S32  pvtLla[3]; // LLA position coordinates in radians, radians, meters.
     S32  pvtPosFilt[3];// Filtered ECEF position coordinates in meters.
     S32  pvtLlaFilt[3]; // Filtered LLA position coordinates in radians, radians,
meters.
     S32  pvtVel[3];// ECEF velocity coordinates in meters per second.
     S32  pvtEnu[3];// ENU velocity coordinates in meters per second.
     S32  pvtVelFilt[3];// Filtered ECEF velocity coordinates in meters per
```



```
second.
     S32  pvtEnuFilt[3];// Filtered ENU velocity coordinates in meters per second.
     S32  pvtBias;  // Filtered clock bias in meters.
     S32  pvtDrift; // Filtered clock drift in meters per second.
     S32  pvtPdop;  // PDOP of fix.
     U32  pvtSigmaPos;// Accuracy of filtered position in meter.
     U32  pvtSigmaVel; // Accuracy of filtered velocity in meters per second.
     U32  pvtSigmaBias;// Accuracy of filtered bias in meter.
     U32  pvtSigmaDrift;// Accuracy of filtered drift in meters per second.
     U32  pvtSigmaHoriz;// Horizontal accuracy of filtered position in meter per
second.
     U32  pvtSigmaVert;// Vertical accuracy of filtered position in meter per
second.
     U32  pvtSpeed; // Horizontal speed in meter per second.
     S32  pvtClimb; // Vertical speed in meter per second.
     S32  pvtDirection;// Direction of user movement in radians.
     } erPvtStruct;
```

Sample Application

```
static osSerialStruct sioDebug;
osSemaphoreStruct debugSema;
/**
 * Program main thread routine.
 */
OS_THREAD_FUNC_RT mainThread(OS_THREAD_FUNC_ARG) {
    osInitSemaphore(&debugSema);
    erStartClient();
    while (1) {
        osSleep(1000);
        if (osGetKey() == 'q') {
            erStopClient();
            break;
        }
    }
   OS_THREAD_FUNC_RTRN(0);
}

/**
 * Program main routine.
 */
void main(int argc, char *argv[]) {
    int comPort;
    erAidingOptionsStruct aid;

    comPort = 1;// Specify COM  port to be used.
    aid.aidProtocol = 0;// Specify aiding protocol to be used,
                        //     0 = autonomous.
    erSetAidingOptions(aid);
    osStartThread(mainThread,0,NULL);
```



```
    while(1) osSleep(1000);
}
/**
 * Output data over serial IO / stdout
 */
void bmOutput(char *line) {
    int j;
    osTakeSemaphore(&debugSema);

    for (j = 0; j < (int)strlen(line); j++) {
        osPutSerial(&sioDebug, line[j]);
    }
   osDropSemaphore(&debugSema);
}
/**
 * This function will be called by the Master when
 * PVT data is available.
  */
void erProvidePvt(erPvtStruct pvt) {
    static long startTime = 0;
    long sysTime = (long)((osGetMsecTimer()+500)/1000);
    char src[4];
    char rmc[80];
    char out[80];
    if (startTime == 0) startTime = sysTime;
    if (pvt.pvtFixSource == 0) strcpy(src,"EST");
    else strcpy(src,"FIX");

    sprintf(out,"%5u %10u %8u  %10d %10d %10d [%s]\r\n",
       sysTime-startTime,pvt.pvtGpsTime,pvt.pvtFixTime,
       pvt.pvtPosFilt[0],pvt.pvtPosFilt[1],pvt.pvtPosFilt[2],src);
    bmOutput(out);
}
```

NMEA Output

The data internally available in the receiver can also be put out in NMEA0183 format. Adding the following lines to erProvidePvt() in the sample code above will put out $GPRMC sentences in addition.

```
// Format NMEA RMC sentence.
erGetNmeaRmc(&pvt, rmc);
bmOutput(rmc);
```

The generated string will look like this

```
$GPRMC,123519,A,4807.038,N,01131.000,E,022.4,084.4,230394,003.1,W*6A
```


8 Ordering Information

The following reference should be used when ordering these devices:

- Opus One Baseband IC: eOP1100B
- Prelude One BiCMOS RF Frontend Chip: ePR1015B
- Navigation software will be provided directly from eRide during design in per the customer's system requirement (Host-CPU and operating system platform)

For further assistance please contact your eRide's regional sales representative.

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