Wireless CPU Q24 Series Customer Design Guideline

Revision: 002

Date: September 2006

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Wireless CPU Q24 Series

Customer Design Guideline

Reference: **WM_PRJ_Q24NG_CDG_002**
Revision: **002**
Date: **September 2006**

Powered by the Open AT® Software Suite

Cautions

This platform contains a modular transmitter. This device is used for wireless applications. Note that all electronics parts and elements are ESD sensitive.

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Web Site Support

General information about Wavecom and its range of products: www.wavecom.com

Specific support is available for the Q24 Classic, Plus, Extended and Auto Wireless CPU: www.wavecom.com/Q24Classic,

www.wavecom.com/Q24Plus,

www.wavecom.com/Q24Extended,

www.wavecom.com/Q24Auto

Carrier/Operator approvals: www.wavecom.com/approvals

Open AT® Introduction: www.wavecom.com/OpenAT

Developer support for software and hardware: www.wavecom.com/forum

Overview

This document gives recommendations and general guidelines to help design a product using the Wireless CPU Q24 Series.

The recommendations include:

- Design rules and typical implementation examples,
- Mechanical constraints,
- PCB layout recommendations,
- Test and download recommendations.

The Wireless CPU Q24 Series is available in four different GSM/GPRS Class 10 quad-band versions:

- Q24 Classic: EGSM 900/1800/850/1900 MHz version with 32 Mb of Flash memory and 16 Mb of PSRAM (32/16), T° range [-20°C / +55°C].
- Q24 Plus: EGSM/GPRS 900/1800/850/1900 MHz version with 32 Mb of Flash memory and 16 Mb of PSRAM (32/16), T° range [-20°C / +55°C].
- Q24 Extended: EGSM/GPRS 900/1800/850/1900 MHz version with 32 Mb of Flash memory and 4 Mb of SRAM (32/4), extended T° range.
- Q24 Automotive: EGSM/GPRS 900/1800/850/1900 MHz version with 32 Mb of Flash memory and 4 Mb of PSRAM (32/4), extended T° range.

This version is dedicated to automotive applications.

For further information about the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

For detailed software programming guides, refer to the documents shown in the "Reference documents" section.

Open AT® Software Suites allow developers to natively execute ANSI C software programs directly on the Wireless CPU.

Document History

Revision	Date	List of revisions	
001	May 2006	Creation (Preliminary version)	
002	September - 2006	First update	

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Table of Figures

1 References

1.1 Reference Documents

For more details, several reference documents may be consulted. The Wavecom reference documents are provided in the Wavecom documents package contrary to the general reference documents, which are not Wavecom owned.

1.1.1 Wavecom Reference Documents

[1] Automotive Environmental Control Plan for Wireless CPU Q24 Series
WM_PRJ_Q24NG_DCP_001

[2] Environmental Control Plan for Wireless CPU Q24 Series
WM_PRJ_Q24NG_DCP_002

[3] Wireless CPU Q24 Series Product Technical Specification
WM_PRJ_Q24NG_PTS_002

[4] Wireless CPU Q24 Series Process Customer Guidelines
WM_PRJ_Q24NG_PTS_003

[5] AT Commands Interface Guide for OS 6.57
WM_ASW_OAT_UGD_0044

[6] AT Commands Interface Guide (Bluetooth)
WM_ASW_BLU_UGD_001

[7] ADL User Guide for Open ATA® V.3.12
WM_ASW_OAT_UGD_006

1.1.2 General Reference Documents

[8] "I²C Bus Specification", Version 2.0, Philips Semiconductor 1998

[9] ISO 7816-3 Standard

1.2 Abbreviations

Abbreviation	Definition
AC	Alternating Current
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AF	Audio-Frequency
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CAN	Controller Area Network
CB	Cell Broadcast
CEP	Circular Error Probable
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CS	Coding Scheme
CTS	Clear To Send
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DCS	Digital Cellular System
DR	Dynamic Range
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
E-GSM	Extended GSM
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
EMS	Enhanced Message Service

Abbreviation	Definition
EN	ENable
ESD	ElectroStatic Discharges
FIFO	First In First Out
FR	Full Rate
FTA	Full Type Approval
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communications
HR	Half Rate
I/O	Input / Output
LED	Light Emitting Diode
LNA	Low Noise Amplifier
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MO	Mobile Originated
MT	Mobile Terminated
na	Not Applicable
NF	Noise Factor
NMEA	National Marine Electronics Association
NOM	NOMinal
NTC	Négative Temperature Coefficient
PA	Power Amplifier
Pa	Pascal (for speaker sound pressure measurements)
PBCCH	Packet Broadcast Control CHannel

Abbreviation	Definition
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PFM	Power Frequency Modulation
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
RFI	Radio Frequency Interference
RHCP	Right Hand Circular Polarization
RI	Ring Indicator
RST	ReSeT
RTC	Real Time Clock
RTCM	Radio Technical Commission for Maritime services
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Wireless CPU
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
SPK	SPeaKer
SRAM	Static RAM
TBC	To Be Confirmed
TDMA	Time Division Multiple Access
TP	Test Point
TVS	Transient Voltage Suppressor
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter

Abbreviation	Definition
USB	Universal Serial Bus
USSD	Unstructured Supplementary Services Data
VSWR	Voltage Standing Wave Ratio

2 General Description

2.1 General Information

The Wireless CPU Q24 Series are self-contained EGSM/GPRS 900/1800 and 850/1900 quad-band Wireless CPUs with the following characteristics.

Note:

Only the Q24 classic is limited to GSM (GPRS not supported).

2.1.1 Overall Dimensions

Completely shielded:

- Length: 58.4 mm
- Width: 32.2 mm
- Thickness: 3.9 mm
  - Excluding shielding legs
  - 6.2 mm for Q24 Automotive which offers a MMS or UFL connector on the top side
- Weight:<11 g (12g for Q24 Automotive)

2.1.2 GSM/GPRS Features

- 2-Watt EGSM 900/GSM 850 radio section running under 3.6 volts
- 1-Watt GSM1800/1900 radio section running under 3.6 Volts
- Hardware GSM/GPRS class 10 capable (except the Wireless CPU Q24 Classic)

2.1.3 Interfaces

- Complete interfacing is through a 60-pin connector:
  - SPI and I^2C bus interfaces
  - Keyboard interfaces
  - Two serial links interfaces (UART1 and UART2)
  - 3V/1.8V SIM interface
  - GPIOs
  - Activity status indication interface
  - Analog to digital converter
  - Analog audio
  - Buzzer interface
  - Battery charging interface
  - External interrupt
  - Power supply interface

- o Back-up battery interface
- Optional SIM Card holder

2.1.4 External RF Connection Interfaces

The Wireless CPU Q24 Series are available with different external RF connection configurations:

Product reference	UFL	UFL or MMS	Antenna pad	IMP
Position	bottom side	top side	top side	bottom side
Q24 Classic	X		X	X
Q24 Plus	X		X	X
Q24 Extended	X		X	X
Q24 Automotive		X	X	X

2.1.5 SIM CARD Holder

The Wireless CPU Q24 Series are available with a SIM CARD holder on the TOP:

	SIM interface location	
Product reference	60-pin connector	Optional SIM holder
Q24 Classic	X	X
Q24 Plus	X	X
Q24 Extended	X	
Q24 Automotive	X	

Caution:

- The Wireless CPU Q24 Series does not allow two SIM Cards to be connected at the same time.
- If a Wireless CPU Q24 Plus or Extended is used with a SIM CARD holder at the top, It is mandatory to avoid the SIM interface through the 60-pin General Purpose Connector (GPC).

2.1.6 Green Policy

The Wireless CPU Q24 Series are compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment). Directive 2002/95/EC, which sets limits for the use of certain restricted hazardous substances.

This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE)".

2.2 Functional Architecture

The global architecture of the Wireless CPU Q24 Series is shown below:

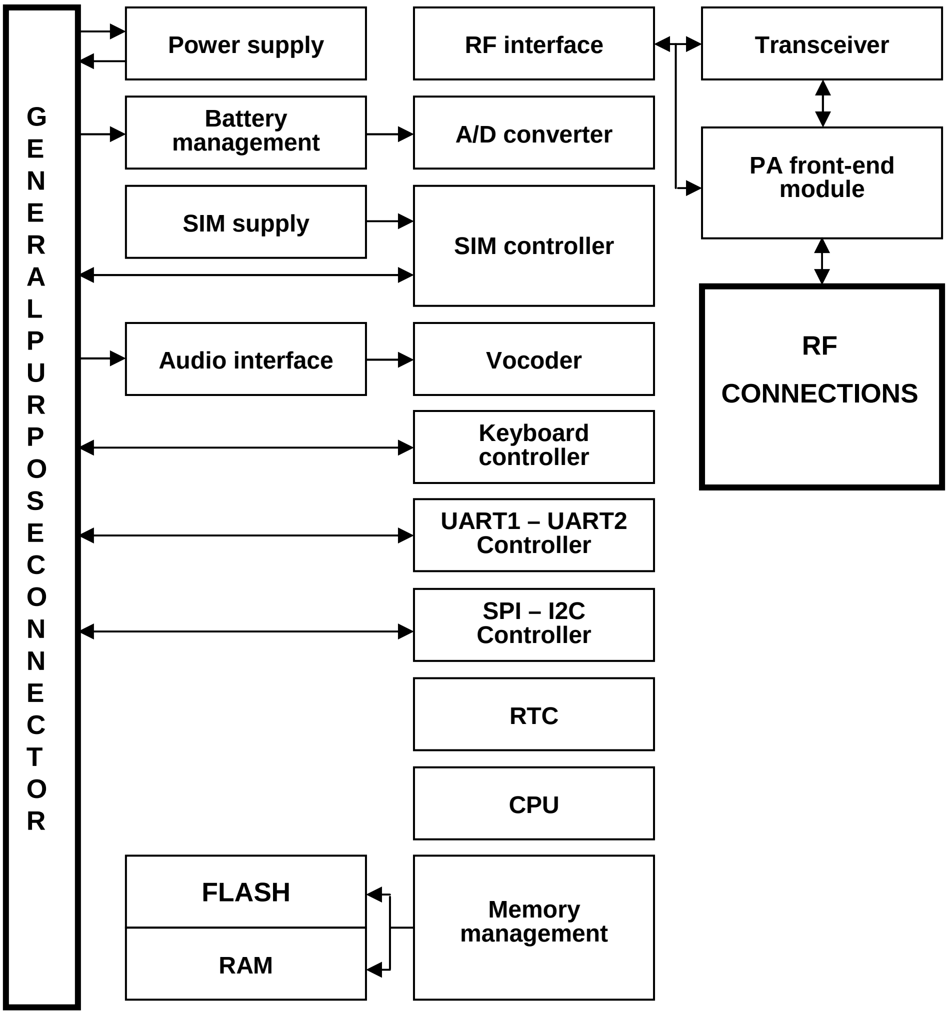


Figure 1: Functional architecture

3 Power Supply Recommendations

3.1 Ground Connections Recommendations

The ground connections of the Wireless CPU Q24 Series are made through the four legs of the shielding.

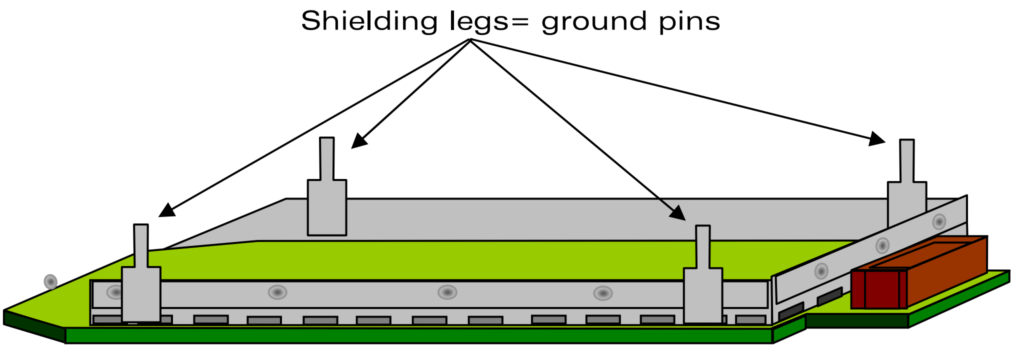


Figure 2: Q24 Series and ground connections

- A complete ground plane must connect the four legs of the Wireless CPU.
- Connections between other ground planes must be made either with vias or µvias.
- The ground pins must be soldered on both sides of the PCB. This helps speed up the heat dissipation process.

Caution:

To avoid coupling effect with radiated noise, it is recommended to avoid layout at the top layer of the application located under the Wireless CPU.

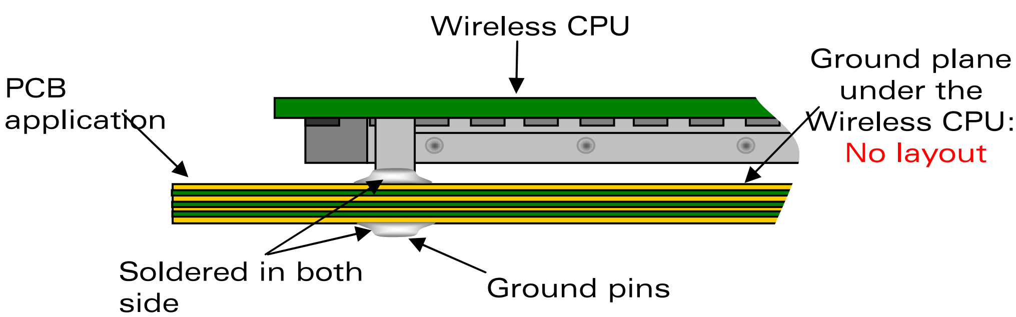


Figure 3: Shielding legs connections

3.2 Power Supply Generalities

The power supply is one of the key factors in the design of a GSM terminal.

The VBATT voltage limits must be at any time: 3.2V <VBATT< 4.5V

The worst condition is during the burst period transmission, when current consumption is at its highest. During this period, the VBATT voltage is minimum:

- The output voltage of the power supply drops.
- Voltage drop is present between the power supply output and the Wireless CPU supply pins (VBATT).

3.3 Voltage Versus Distance

Depending on the distance between the power supply and the Wireless CPU, behavior is as follows:

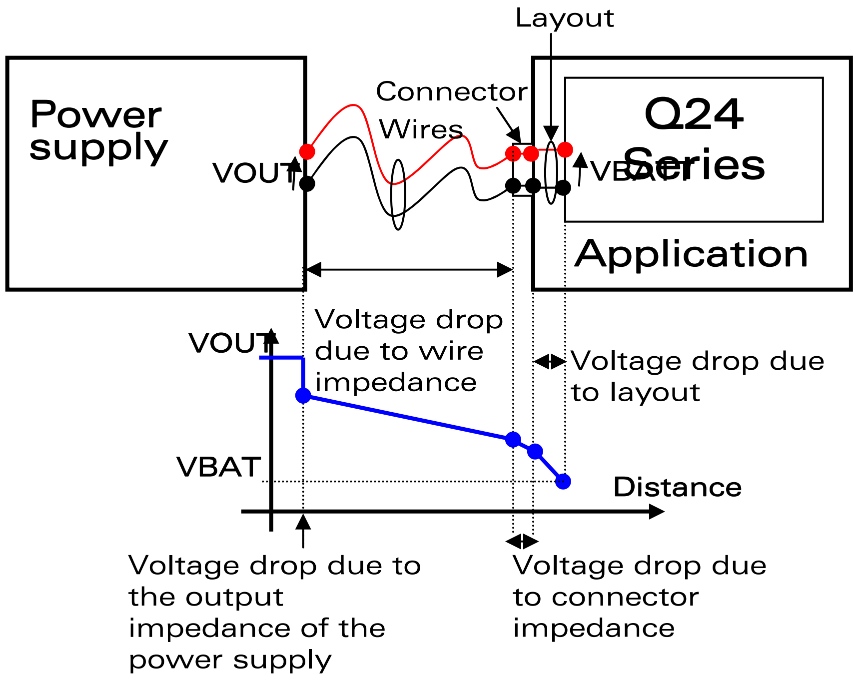


Figure 4: Voltage drop versus distance

For further information about the power supply of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

Caution:

- The total impedance (power supply output impedance+ wires+ connectors+ layout) must be below 150mΩ.
- The design of the supply path between the Wireless CPU and the power supply must take into account the forward and return paths.

Example:

Using a Li-Ion battery to supply a Wireless CPU, the total impedance of the supply track must be divided as follows:

- Cell impedance ≅70 mΩ
- PCM impedance ≅50 mΩ
- Battery connector ≅ 20 mΩ
- PCB supplying track ≅10 mΩ (forward and return path)

Totally: Cell +PCM + connector+ supplying track ≅ 150mΩ

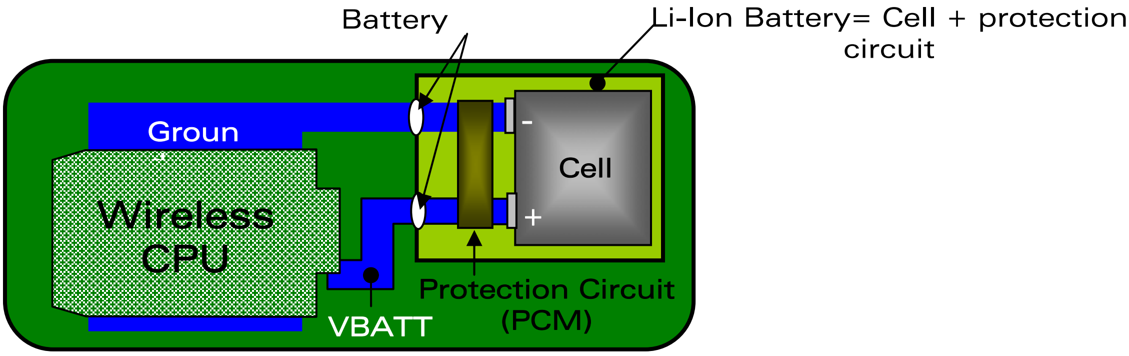


Figure 5: Typical Li-Ion battery connection

3.4 Voltage Versus Time

According to time, the voltage supplying a GSM terminal varies as follows:

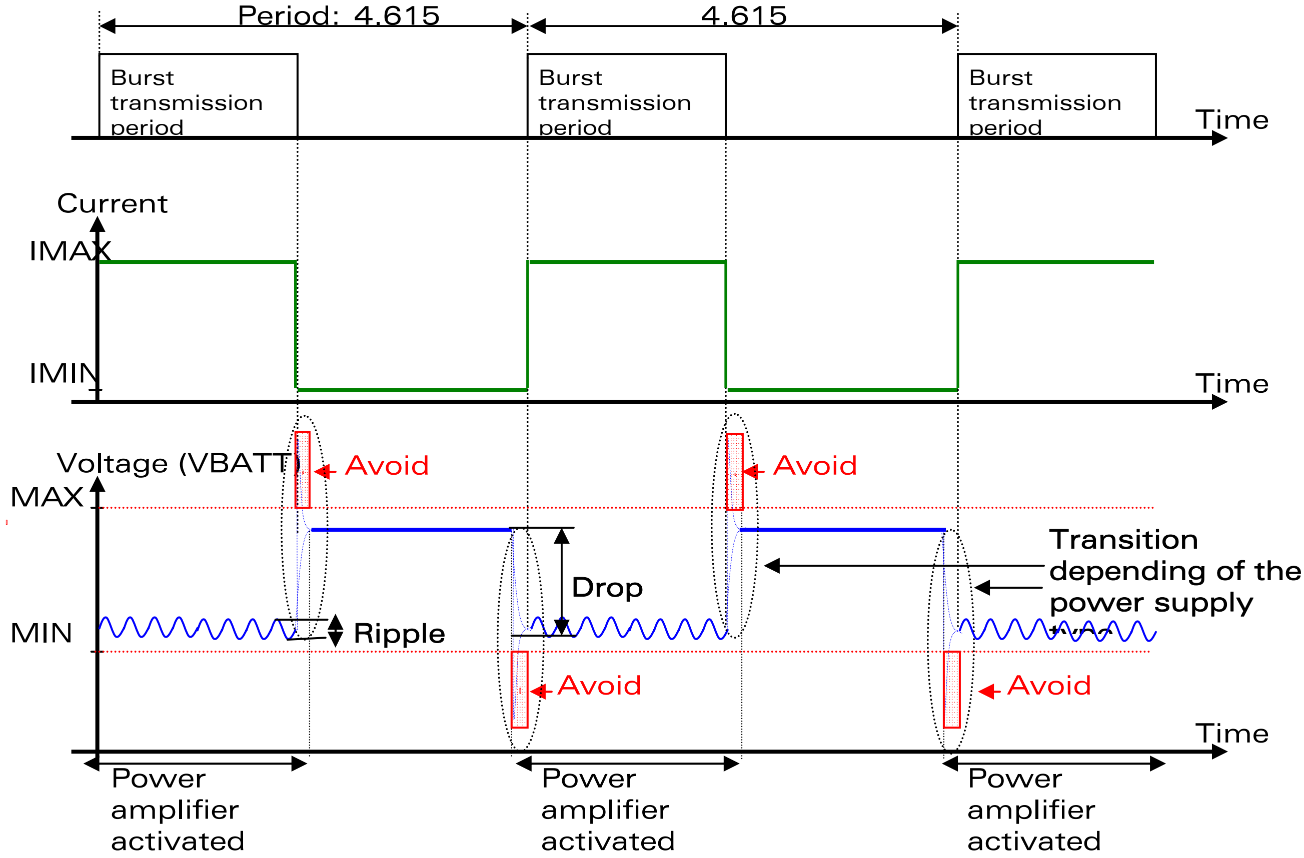


Figure 6: Voltage drop versus time

Note:

The burst transmission period depends on the transmitted burst:

577µs for one transmit burst and **1154 µs** for 2 transmitted bursts (GPRS class 10)

Caution:

The waveform of the voltage may affect the performance of the Wireless CPU:

- If the drop is too high, the VBATT voltage reaches the minimum admissible limit ($VBATT_{MIN}$=3.2V).
- If VBATT<$VBATT_{MIN}$ at any time, the Wireless CPU powers OFF automatically.

- If the power supply time response is too long, transients may appear.

  These transients may make the voltage:

  - higher than the maximum admissible limit ($VBATT_{MAX}$=4.5V)
  - lower than the minimum admissible limit ($VBATT_{MIN}$=3.2V)

- If VBATT>$VBATT_{MAX}$ at any time, the Wireless CPU may be damaged.
- If the transition time is too long, a high ripple of voltage may appear at the beginning of the burst transmission period; this high ripple may directly affect radio performance (phase error, modulation spectrum).
- Depends on the ripple frequency and amplitude, the RF performance may be affected (mainly the modulation spectrum).

3.5 Design Recommendation

The key aspects of power supply design are:

- Quality of the power supply (impedance and transient).
- Supply track design between the power supply and the supply pins (VBATT) of the Wireless CPU.
- Decoupling capacitors.

3.5.1 Power Supply Selection

The power supply must have:

- A low output impedance
- A fast time response
- A good ripple rejection according to the Wireless CPU specification
- A capacity to deliver a high peak of current in a short time (2A)

There are different types of power supplies; some of these are not suitable for a GSM application because of noise generation, which may affect the RF performance.

Type of power supply	Power supply type and general behavior	Recommendation
Linear Voltage regulator	Good regulation	Recommended if • Good ripple rejection • Low drop of voltage • Ability to deliver a high peak of current (2A typ)
Switching power supply with an embedded Pulse Width Modulation system (PWM)	Except the switching frequency, which may affect the RF performance (mainly the modulation spectrum), the behavior is good.	Recommended if • Good ripple rejection • Low voltage drop • Ability to deliver a high peak current (2A typ) • If the switching frequency is not a multiple of 100kHz
Switching power supply with an embedded Pulse Frequency Modulation system (PFM)	The constraint on the PFM is the switching frequency, which varies according to the load. "The higher the sink current, the higher the switching frequency"	Avoid

3.5.2 Design of the Supply Track

To avoid any supply track related problems it is better to:

- Dedicate a track from the power supply output to the supply pins of the Wireless CPU.

  -some other components connected to this track may also be sensitive to the voltage drop due to the Wireless CPU.

  -other devices using the same power supply may generate noise
- Place the power supply output as close as possible to the supply pins of the Wireless CPU.
- Consider the output DC impedance of the power supply, DC impedance of the PCB layout, and the connectors and wires connecting the power supply to the Wireless CPU (forward and return path).

3.5.2.1 Voltage Drop and Impedance

⚠ Caution:

The voltage drop may affect Wireless CPU performances if too high, but the maximum admissible voltage drop depends on its waveform. To guarantee the

Wireless CPU performance, irrespective of the waveform, the voltage drop must stay within 300mV.

Under a 300mV maximum voltage drop with a current of 2A, the DC impedance of the tracks connecting the power supply output to the supply pin of the Wireless CPU may be as shown below:

300mV/ 2A=150mΩ (return + forward path).

Note:

During a transmit burst, Wireless CPU nominal current is 1.4A only.

To design the Wireless CPU power supply track with a margin, a target of 2A is recommended.

Information on connector DC impedance and power supply DC output impedance is available in the datasheet.

In general, the constraints on the wires are:

- They are not shielded against radiated noise (TDMA noise, Digital noise)
- They do not support 2A current

3.5.2.2 PCB and Supply Track

Designing a supply track on a PCB requires special care with a GSM application.

- The width of the track must be wide enough to decrease the voltage drop as far as possible
- The track must be surrounded by ground (through either µvias or a ground plane) to avoid coupled disturbances (Digital noise, RF noise)

In general, Wavecom recommends a supply track width>3mm as being sufficient.

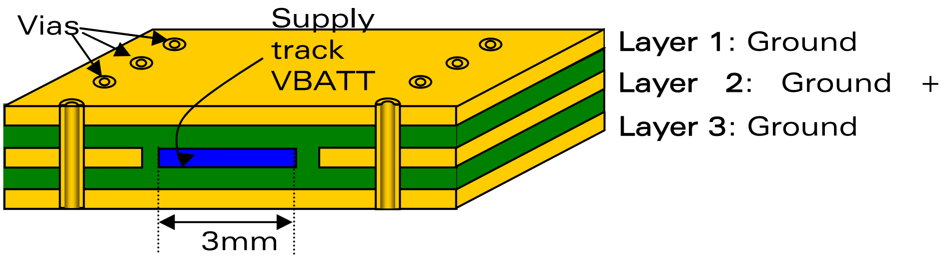


Figure 7: VBATT supply track and PCB layout

Caution:

The supply track must connect the 6 supply pins of the Wireless CPU:

- Pins 55, 57, 58, 59, and 60 for VBATT
- Pin 11 for VDD

If the ground track between the Wireless CPU and the power supply is a ground plane, it must:

- Not be parceled out
- Connect the four legs of the Wireless CPU.

3.5.3 Decoupling capacitors

Two decoupling capacitors (33pF and 10µF with ceramic technology), close to the Wireless CPU supply pins are recommended.

The purpose is to avoid EMI/RFI EMI / RFI problems.

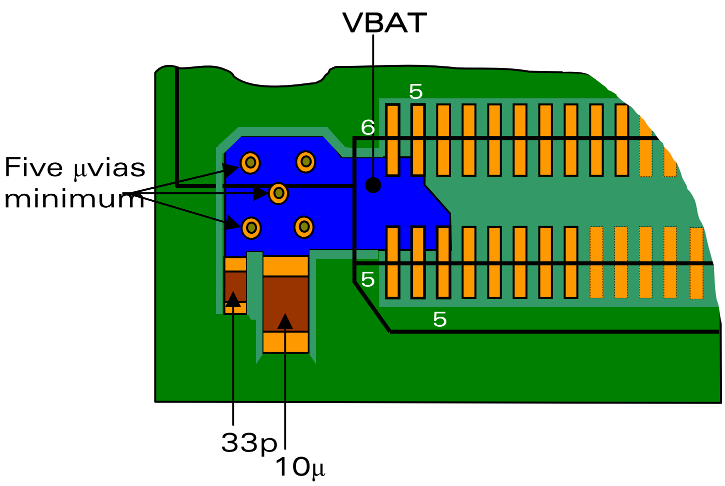


Figure 8: VBATT and decoupling capacitors

4 Power Consumption

The Wireless CPU Q24 Series support different power consumption modes:

Working modes	Comments
ALARM mode	The Wireless CPU is in OFF mode, when an ALARM occurs, the Wireless CPU wakes-up automatically.
FAST idle mode	The Wireless CPU is synchronized with an RF GSM/GPRS network. The internal 26 MHz of the Wireless CPU is constantly active.
SLOW idle mode	The Wireless CPU is synchronized with an RF GSM/GPRS tester. The internal 26 MHz of the Wireless CPU is not constantly active.
FAST Standby mode	The SIM and Radio interface are deactivated via AT command or Open AT API: -The embedded open AT application is running, -The serial port remains active (AT commands are available). The internal 26 MHz of the Wireless CPU is constantly active
SLOW Standby mode	This mode is similar to FAST Standby mode. All the features are disabled (no GSM, no GPRS, no SIM and no serial port) The internal 26 MHz of the Wireless CPU is not constantly active.
Communication mode	A GSM/GPRS communication is established with an RF GSM/GPRS network.

The power consumption depends on the configuration used.

To enable and find the measurement results given in the Product Technical Specification [3], it is recommended to follow the procedure described in the table below:

<u>Note:</u>

Each power consumption mode may be enabled by using an AT command.

Working modes	Measurement conditions Note The settings which may change with the GSM/GPRS network are shown in blue
ALARM mode	AT+CALA="yy/mm/dd, hh:mm" is used to set an alarm and the Wireless CPU may be switched OFF using AT+CPOF. Once the alarm has elapsed, the Wireless CPU starts automatically. This method is used to save power when required. -If the VBATT voltage is totally disconnected from the Wireless CPU, a back-up battery is needed to connect to the Wireless CPU. Notes: -To set the time inside the module, the AT command AT+CCLK="yy/mm/dd,hh:mm:ss" may be used -To check the time: AT+CCLK? -To avoid extra power consumption, when the Wireless CPU is in ALARM mode, do not apply any voltage in the UART1 interface.
FAST idle mode	Paging every 9 multi-frames (every 2 seconds)
	Paging every 2 multi-frames (every 0.5 seconds)
SLOW idle mode	AT+W32K=1 and the signal CT108-2/DTR1 must perform a rise edge (0V to 2V8). Paging every 9 multi-frames (every 2 Seconds) Note: If the CT108-2/DTR1 signal perform a fall edge, the FAST idle mode is activated.
	AT+W32K=1 and the signal CT108-2/DTR1 must perform a rise edge (0V to 2.8V) Paging every 2 multi-frames (every 0.5 Seconds) Note: If the CT108-2/DTR1 signal performs a fall edge, the FAST idle mode is activated
FAST Standby mode	-The AT command "AT+WBHV=1, 1" is send to the Wireless CPU. -The Wireless CPU is re-started in order to take this new behavior into account. During the reset, the Wireless CPU is initialized without the GSM stack or network registration. -Current consumption is measured after the Wireless CPU is re-started Notes: -To deactivate this mode, AT+WBHV=1, 0 must be used and the Wireless CPU must be re-started. -If any data is to be transmitted through the network, the RF must be activated first. The GSM/GPRS communication may then be made to send data.

Working modes	Measurement conditions Note The settings which may change with the GSM/GPRS network are shown in blue	
SLOW Standby mode	-The AT command "AT+WBHV=1, 2" is sent to the Wireless CPU and the signal CT108-2/DTR1 must perform a fall edge (0V to 2.8V). -The Wireless CPU is re-started in order to take this new setting into account. During the reset, the Wireless CPU is initialized without the GSM stack or network registration. Note: To de-activate this mode, the CT108-2/DTR1 must perform a fall edge (2V8 to 0V), then, the AT command AT+WBHV=1, 0 must be sent and the Wireless CPU must be re-started (power-OFF or reset).	
Communication mode	GSM mode	GSM850 @PCL5 and PCL19
		GSM900 @PCL5 and PCL19
		DCS1800@PCL0 and PCL15
		PCS1900@PCL0 and PCL15
	GPRS Class 8 Note: GPRS attachment with AT+CGATT=0,0 or for automatic attachment AT+WGPRS=0,0	GPRS850 1TX/4RX slot @Gamma 3 and Gamma 17
		GPRS900 1TX/4RX slot @ Gamma 3 and Gamma 17
		GPRS1800 1TX/4RX slot @ Gamma 3 and Gamma 18
		GPRS1900 1TX/4RX slot @ Gamma 3 and Gamma 18
	GPRS Class 10 Note: GPRS attachment with AT+CGATT=0,0 or for automatic attachment AT+WGPRS=0,0	GPRS850 2TX/4RX slot @ Gamma 3 and Gamma 17
		GPRS900 2TX/3RX slot @ Gamma 3 and Gamma 17
		GPRS1800 2TX/3RX slot @ Gamma 3 and Gamma 18
		GPRS1900 2TX/3RX slot @ Gamma 3 and Gamma 18

5 Interfaces

Some of the Wireless CPU Q24 Series interface signals are multiplexed, in order to limit the total number of pins.

This architecture is more flexible, but imposes some restrictions.

Example:

If the SPI bus and I^2C bus are multiplexed and if the SPI bus is used, the I^2C bus is not available.

Caution:

To power-ON the Wireless CPU Q24 Series correctly and to avoid damage, all external signals must be inactive when the Wireless CPU Q24 Series is OFF.

5.1 Digital I/O and Peripheral Implementation

All digital I/O comply with 3 volts CMOS.

For further information on the Digital I/O of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

To interface the Wireless CPU digital signals with other logics, the possibilities are as follows:

- 3.3 V logic: some serial resistors (more than 11kΩ) may be added to the tracks,
- For higher voltage logics, a resistor bridge or a level shifter may be used.

5.2 Serial Interface

For further information on the Serial interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

Note:

The SPI or I^2C bus interface of the Wireless CPU supports only a master mode, with the Wireless CPU being the master.

5.2.1 SPI Bus

The SPI bus includes:

- Pin 10: A CLK signal (SPI_CLK)
- Pin 8: An input /Output signal (SPI_IO)
- Pin 28: An activation signal (SPI_EN)

These three signals comply with the SPI bus standard.

Note:

By using another activation signal (pin 26, SPI_AUX), it is possible to connect two devices using a SPI bus.

5.2.2 I²C Bus

The I²C interface includes:

- Pin 10: A CLK signal (SCL)
- Pin 8: A DATA signal (SDA)

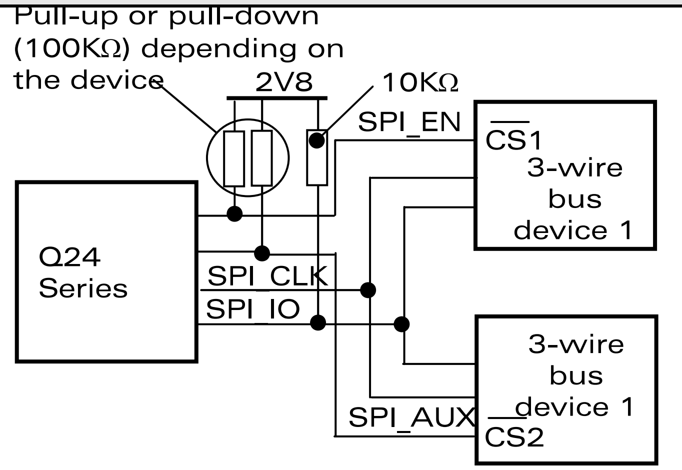
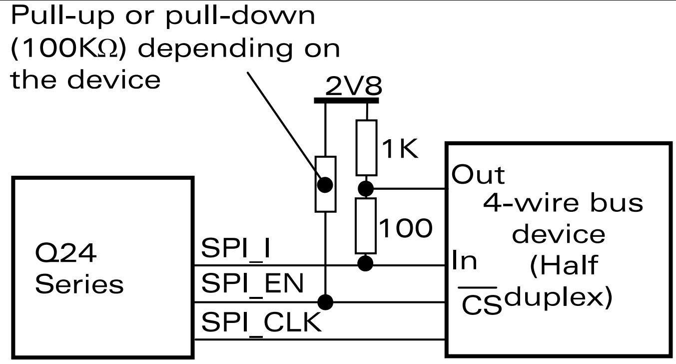
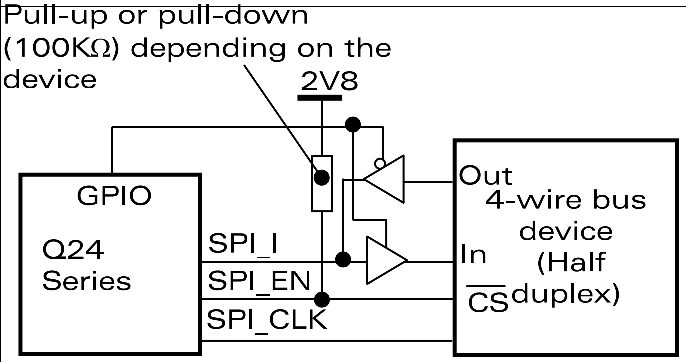
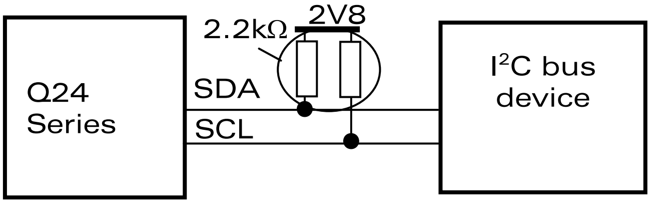
The two signals are multiplexed with the SPI bus. They comply with the I²C bus standard.

5.2.3 SPI and I²C Bus Implementation

The SPI bus of the Wireless CPU Q24 Series is designed with three wires.

It is also possible to connect a device with a 4-wire SPI bus interface working in half or full duplex data rate by using external hardware.

The table below summarizes the possibilities:

Type	Schematic example	Comments
3-wire SPI bus		Using two activation signals (SPI_EN and SPI_AUX), it is possible to connect two devices.
Adaptation of a half duplex device 4-wire SPI bus		As per definition, if the device is half duplex, the input (In) and output (Out) do not work at the same time.
Adaptation of a full duplex device 4-wire SPI bus		As per definition, if the device is full duplex, the input (In) and output (Out) may work at the same time. Using two buffers may avoid the device reading the information sent by itself (data corruption).
I²C bus		Typical implementation of the I²C bus

5.3 Keyboard Interface

For a total of 25 keys (5 rows x 5 columns), the keyboard interface provides 10 connections:

- 5 rows (ROW0 to ROW4) and
- 5 columns (COL0 to COL4).

Signals	Pin number	Description
ROW0	13	Row scan
ROW1	15	Row scan
ROW2	17	Row scan
ROW3	19	Row scan
ROW4	21	Row scan
COL0	23	Column scan
COL1	25	Column scan
COL2	27	Column scan
COL3	29	Column scan
COL4	31	Column scan

The scanning is digital, and the debouncing is performed in the Wireless CPU. No discrete components such as R, C (Resistor, Capacitor) are needed.

For further information on the keyboard interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

A typical implementation is as shown in Figure 9.

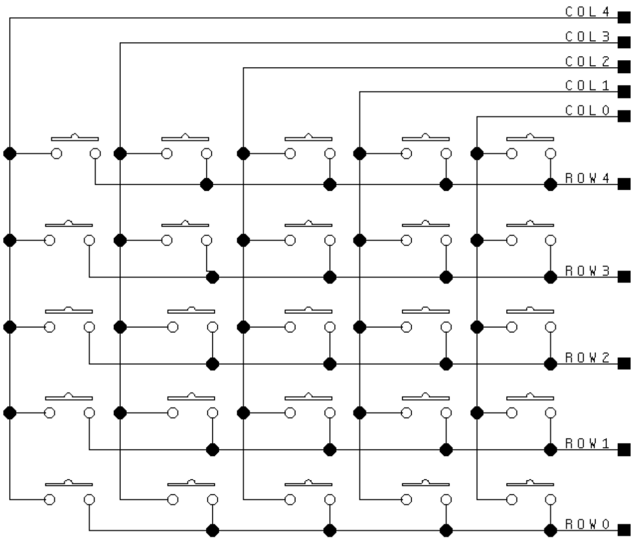


Figure 9: Example of Keyboard implementation

5.4 Main Serial Link (UART1)

5.4.1 General Description

A flexible 6/8-wire serial interface is available complying with V24 protocol signaling, but not with V28 (electrical interface) due to a 2.8 volt interface.

The signals are:

- Pin 39: TX data (CT103/TXD1)
- Pin 32: RX data (CT104/RXD1)
- Pin 30: Request To Send (CT105/RTS1)
- Pin 37: Clear To Send (CT106/CTS1)
- Pin 36: Data Set Ready (CT107/DSR1)
- Pin 34: Data Terminal Ready (CT108-2/DTR1)
- Pin 51: Data Carrier Detect (CT109/DCD1).
- Pin 54: Ring Indicator (CT125/RI).

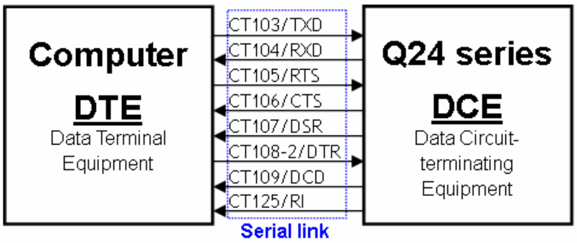


Figure 10: UART1 Serial Link signals

The UART1 serial interface allows a baud rate up to 460800.

For further information on the UART1 interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.4.2 Design Recommendation

- To avoid extra power consumption or malfunction of the Wireless CPU, when the Wireless CPU is either in OFF mode or ALARM mode, do not apply any voltage to the UART1 signal.
- For download and debugging purposes, It is mandatory to have an access to the signals TXD1, RXD1, RTS1, and CTS1 (through test points for example).
- Because the signals DTR1, TXD1, and RTS1 are input pins of the Wireless CPU, irrespective of the application, it is mandatory to connect a pull-up on these signals (100kΩ to 2V8).
- Depending on the application, some serial link signals are not required:
  - If the application manages only the audio, RXD1 and TXD1 signals are sufficient

- If the application manages some data transfer, it is mandatory to also use RTS1 and CTS1 (using RTS1 and CTS1 avoids data corruption).
- DSR1, DCD1, and RI may be left disconnected if not used; some applications, such as a modem, may require these signals.

Examples:

1-Typical implementation of the UART1 interface with a host interface

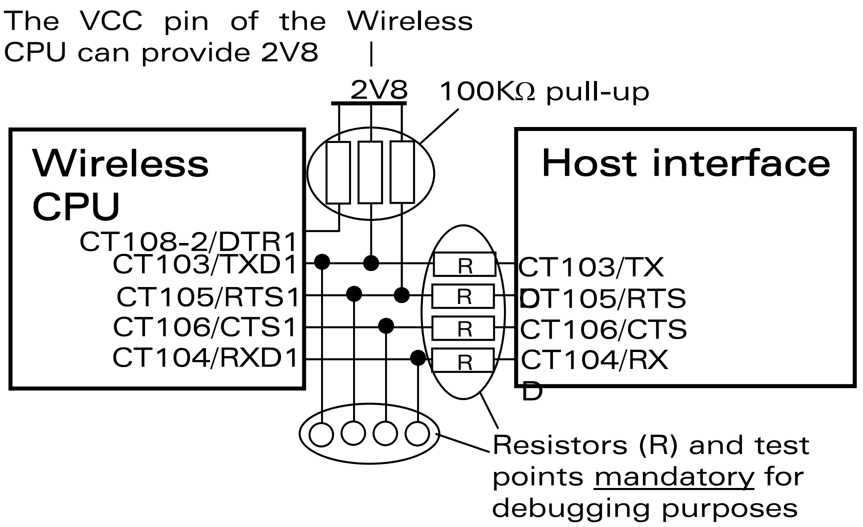


Figure 11: Typical UART1 and host connection

Caution:

- When the Wireless CPU is in OFF mode, an over power consumption may occur if voltages are applied in the serial link.
- The rise and fall time of the reception signals (mainly TXD1) must be less than 200 ns:

  High value serial resistors (R), placed in the serial link signals, may limit the current but, due to the input capacitance of the Wireless CPU (and host interface), if the value is too high, the maximum baud rate becomes limited.

The table below shows an example:

UART1 baud rate	Host interface output voltage		
	<3.1V	3.2V	3.3V
9 600	R < 62 kΩ	6.8 kΩ< R < 62 kΩ	11 kΩ< R < 62 kΩ
19 200	R < 30 kΩ	6.8 kΩ< R < 30 kΩ	11 kΩ< R < 30 kΩ
38 400	R < 15 kΩ	6.8 kΩ< R < 15 kΩ	11 kΩ< R < 15 kΩ
57 600	R < 10 kΩ	6.8 kΩ< R < 10 kΩ	Not supported
115 200	R < 5.1 kΩ	Not supported	Not supported

Note:

For a host interface output voltage of 3.1V, 3.2V or 3.3V, a typical value for the serial resistors is 4K7.

2-Typical implementation of the UART1 interface with a terminal

To interface the UART1 with a terminal (a computer for example), a level shifter may be required.

In the example shown in Figure 12, a level shifter MAX3237E is used.

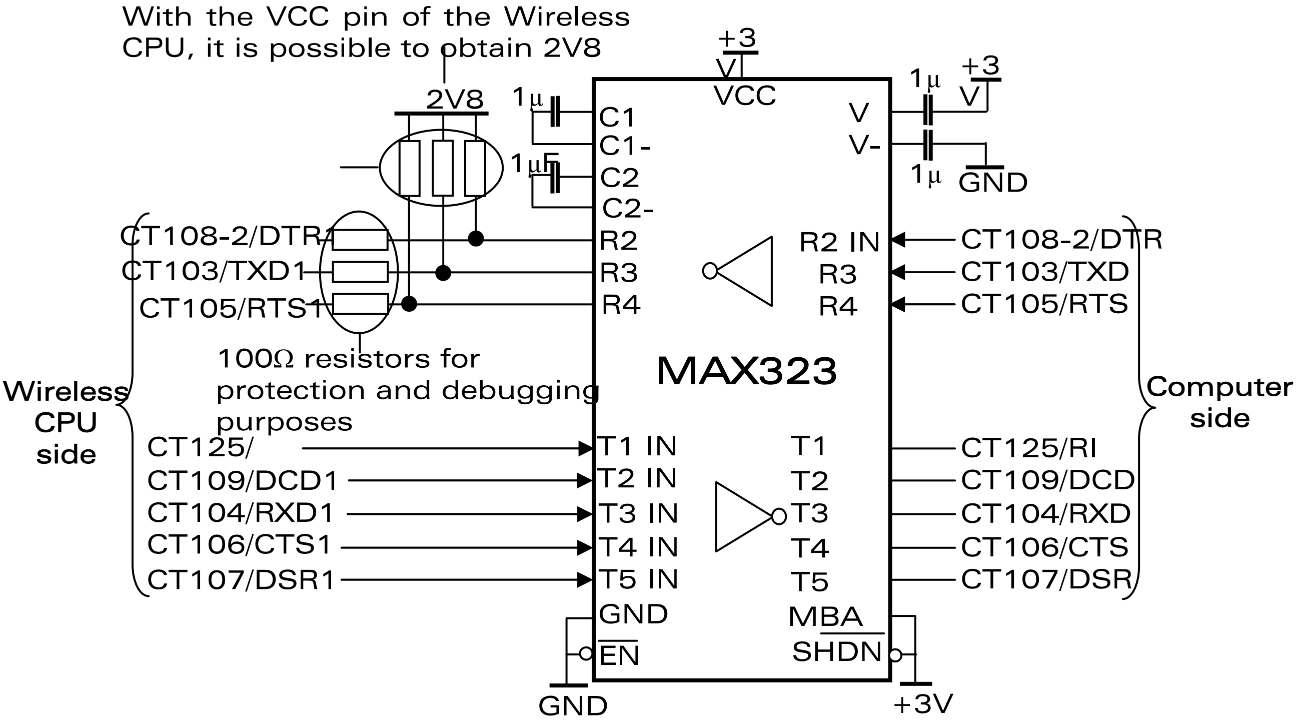


Figure 12: Example of RS232 level shifter implementation

Note:

The MAX3238 is also compatible with the example shown in Figure 12.

5.5 Auxiliary Serial Link (UART2)

5.5.1 General Description

For specific applications, an auxiliary serial interface (UART2) is available on the Wireless CPU Q24 Series.

Example: Bluetooth connectivity.

For more information, see the AT Commands Interface Guide for Bluetooth [6].

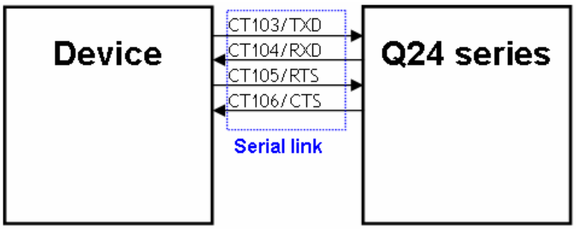


Figure 13: UART2 Serial Link signals

For further information on the UART2 interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.5.2 Design Recommendation

The design recommendations are the same as for UART1.

5.6 SIM Interface

5.6.1 General Description

The following five signals are available:

- Pin 9: SIM power supply (SIM_VCC)
- Pin 5: Reset (SIM_RST)
- Pin 3: Clock (SIM_CLK)
- Pin 7: I/O port (SIM_DATA)
- Pin 50: SIM Card detection (SIM_PRES)

The SIM interface can control a 1V8/3V SIM Card. This interface is fully compliant with the GSM 11.12 recommendations concerning SIM functions.

For further information on the SIM interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

Notes for SIM_PRES connection:

- When not used, SIM_PRES must be tied to 2V8 through a pull-up resistor
- When used, a rising edge means that the SIM Card is inserted whereas a falling edge means that the SIM Card is removed.

5.6.2 Design Recommendation

5.6.2.1 ESD Protections

Low capacitance ESD protections (less than 10 pF) must be connected on SIM_CLK and SIM_DATA signals to avoid any disturbance of the rising and falling edges.

ESD protections are mandatory if the SIM holder is externally accessible. They must be placed as close as possible to the SIM socket.

The following references may be used: ESDA-6V1P6 from ST Microelectronics and AVL5M0220 from AMOTECH.

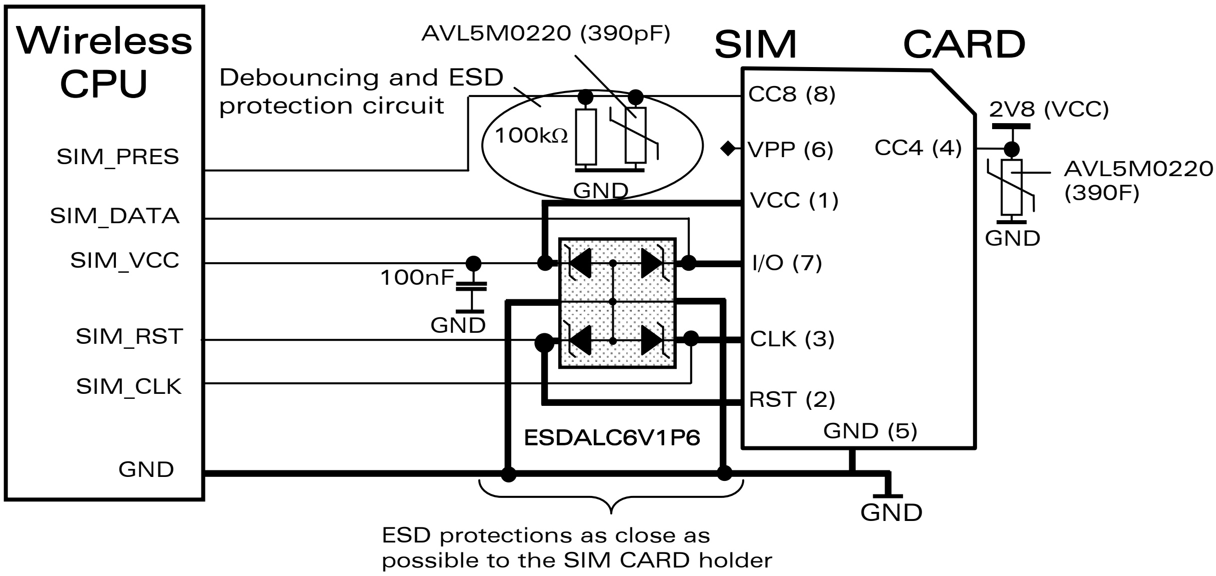


Figure 14: Example of SIM Socket implementation

Note:

The capacitor in SIM_VCC is placed to help the power to counteract spikes in the current consumption of the SIM up to the limits given in the compliance requirement, ensuring that the supply voltage stays in the specified range (Test Case 27.17.2.1.2).

The recommended value is 100nF.

5.6.2.2 SIM CARD Holder

A good SIM CARD holder is one which:

- Prevents electrical disconnection of the SIM CARD
- Avoids direct ESD access to the pin of the SIM CARD holder (a shielded SIM CARD holder is more effective)

5.6.2.3 PCB Layout

Not only is the type of ESD protections important, but also their placement and connection.

ESD protections must be:

- As close as possible to the SIM CARD holder
- Connected to a "good" ground (important to dissipate the ESD energy)
- The track connections from the SIM CARD holder to the ESD protections must be as wide as possible (300 µm minimum)
- It is recommended to decrease the length of the tracks between the Wireless CPU and the SIM connector **as much as** possible (<10 cm maximum).

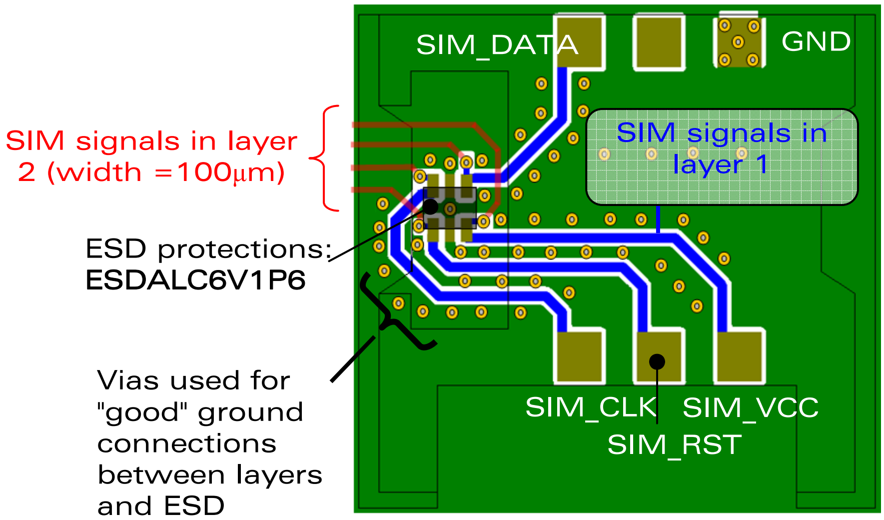


Figure 15: Example of SIM Socket and PCB layout

(Note: No SIM presence used)

Note:

To avoid crosstalk, the SIM signals must be separated by a ground track:

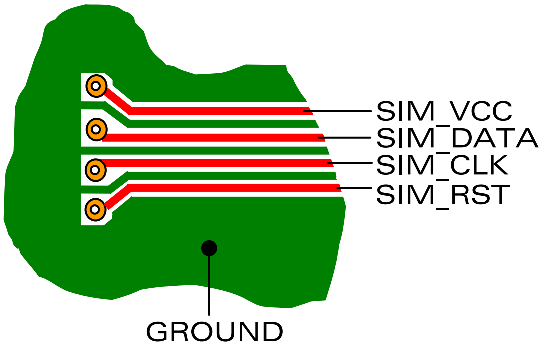


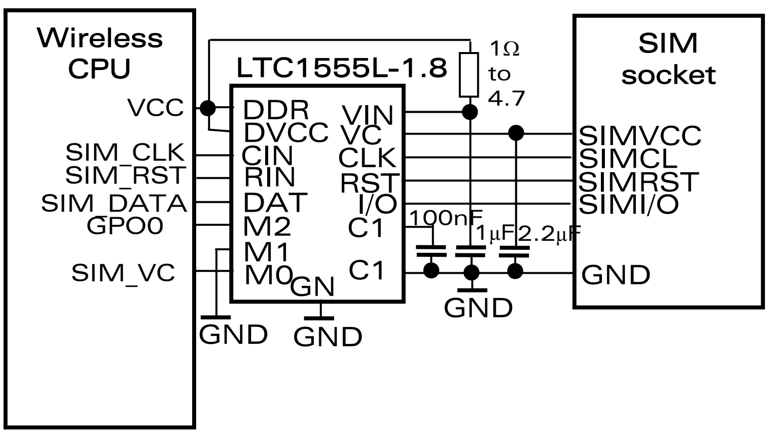
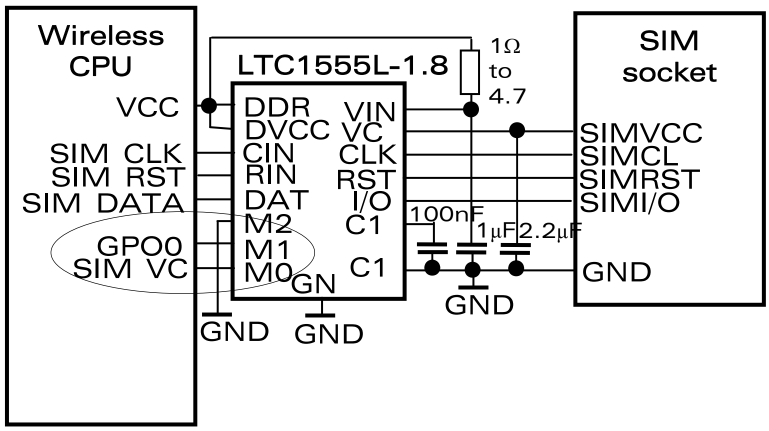
Figure 16: SIM signals and layout

5.6.2.4 SIM Management through an External Level Shifter

Like the WISMO QUICK Q24 family, the Wireless CPU Q24 Series is able to manage the 1V8/3V or 3V/5V SIM CARD by using an external voltage level shifter controlled by the GPO0 output signal (Pin 26).

The choice of an external level shifter device depends on the type of SIM. The Wireless CPU firmware triggers the GPO0 output signal (Pin 26), to automatically set the external SIM driver voltage level to match the voltage level of the SIM inserted.

With a voltage level shifter **LTC1555L-1.8**, the schematics are:

Circuit	Schematic	Logic
SIM 1V8/3V		When SIM_VCC=2V8: • M2=0V→ SIM 3V • M2=2V8→SIM 1V8 __Note:__ • This schematic aims to show the compatibility with the WISMO QUICK Q24 family which is only able to drive a SIM 3V
SIM 3V/5V		When SIM_VCC=2V8: • M1=0V→ SIM 3V • M1=2V8→SIM 5V

5.6.3 Wireless CPU SIM CARD Holder

An optional SIM CARD holder may be used at the top of the Wireless CPU. This SIM CARD holder does not use the SIM_PRES signal. Please refer to Figure 17: SIM CARD holder constraints on next page.

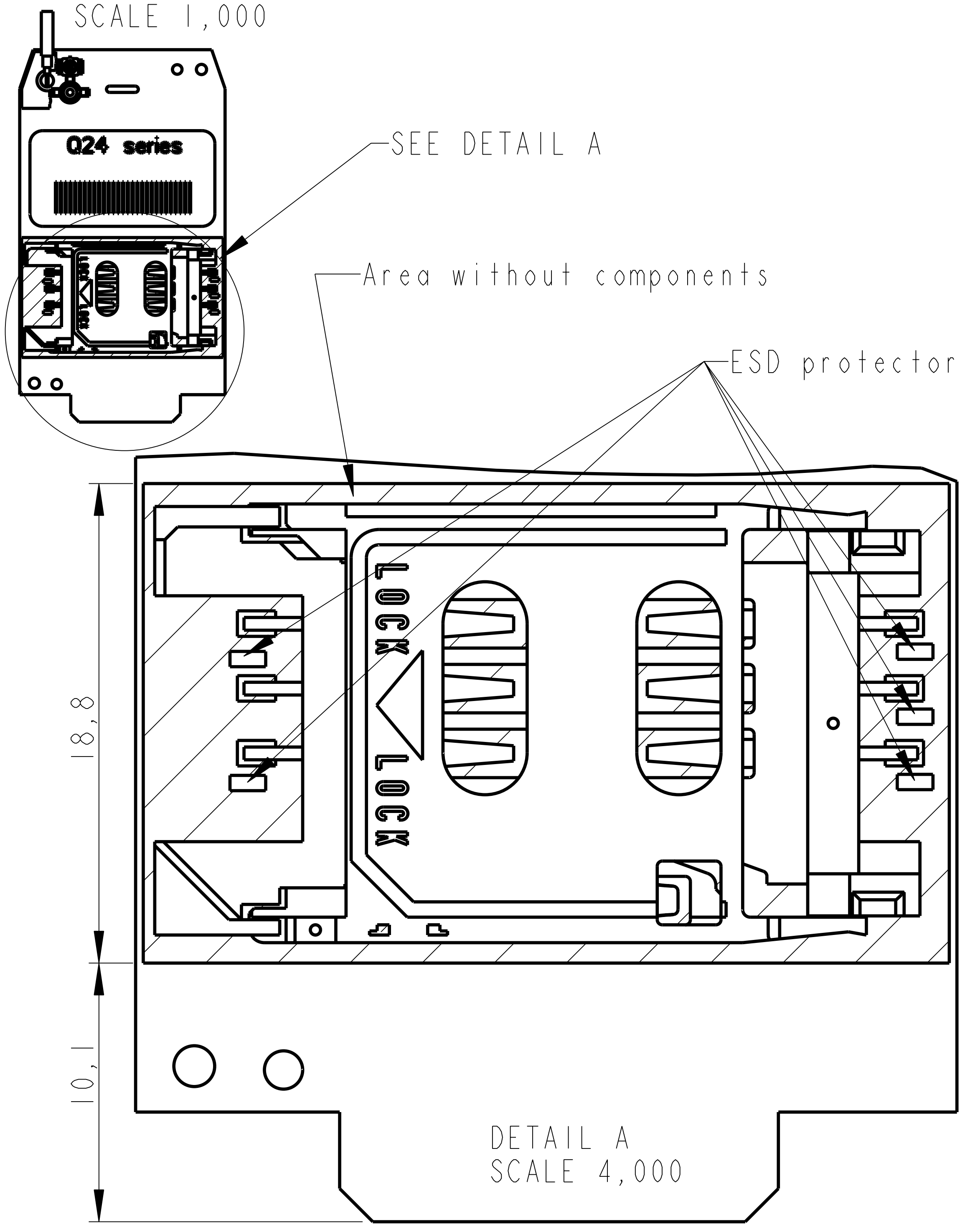
Figure 17: SIM CARD holder constraints (see next page)

Caution:

A Wireless CPU equipped with a SIM CARD holder on top does not allow use of the SIM interface through the 60-pin GPC connector:

- The SIM interface through the 60-pin GPC connector needs to be not connected
- The SIM_PRES signal of the Wireless CPU must be tied to VCC

MODIFICATION	DATE	AUTHOR	RESP.	STATUS	IND
Creation	29/09/06	JPM	ASC	Production	A



ESD PROTECTORS	TOL.GEN.:±0,3		SCALE:1,000
Q24_SERIES		FOLIO : 1/1	
	WM-4-600101-X-017-A		
wavecom			A
PRO/ENGINEER			IND.

Environmental stress applied in the SIM CARD holder may interrupt or damage normal Wireless CPU operation.

The type of environmental stress may be:

- ESD:

  - ESD protections (0402 package) close to the SIM CARD holder aims to decrease the effect of an ESD discharge on the SIM CARD holder.

  - We recommend integration of such ESD protection when designing the mechanical aspects of the application.

- Vibration:

  - A good mechanical design must prevent any direct contact with the SIM

- Humidity

Caution:

Customers are advised to verify that the environmental specifications are compliant with the Wireless CPU Q24 Series.

The application must be qualified with the SIM Card in storage, transportation and operation.

5.7 Analog to Digital Converter (ADC)

Two Analog to Digital Converter are available on the Wireless CPU Q24 Series. These converters are 10-bit resolution, ranging from 0V to 2V8:

- Pin 33: AUXV0 (General Purpose Converter)

  - Used to measure a voltage

- Pin 38: BAT_TEMP (Battery Temperature monitoring or General Purpose Converter)

  - If the Wireless CPU is supplied through a Li-Ion battery, the BAT_TEMP input must be dedicated to the battery temperature measurement (see "Battery Charging Interface").

  - If the Wireless CPU is not supplied by a Li-Ion battery, BAT_TEMP may be used for another purpose similar to AUXV0.

For further information on the ADC interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

Caution:

If AUXV0 and BAT_TEMP are not used, they must be connected to ground.

A typical application may be:

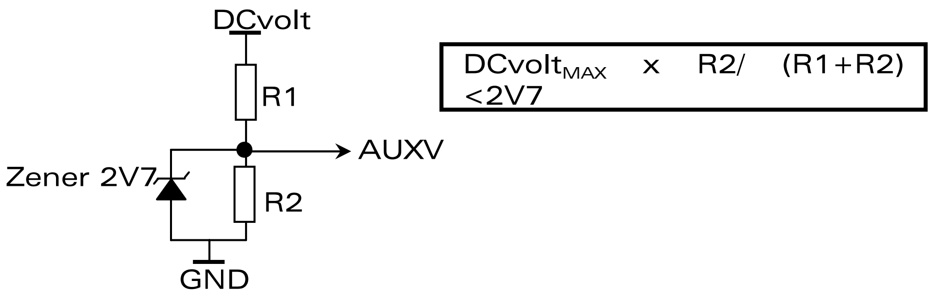


Figure 18: Example of ADC input implementation

5.8 Audio Interface

Two different microphone inputs and two different speaker outputs are supported.

The Wireless CPU Q24 Series also include an echo cancellation feature, which allows hands-free operation.

Caution:

- **When speakers and microphones are exposed to the external environment, it is recommended to add ESD protection on the audio interface lines.**
- **It is important to select an appropriate microphone, speaker and filtering components to avoid TDMA noise.**

For further information on the Audio interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.8.1 Recommended Microphone Characteristics

- The impedance of the microphone must be around 2 kΩ.
- Sensitivity from -40dB to –50 dB.
- SNR > 50 dB.
- Frequency response compatible with the GSM specifications.
- To suppress TDMA noise, it is highly recommended to use microphones with two internal decoupling capacitors:

  - CM1=56pF (0402 package) for the TDMA noise coming from the demodulation of the GSM 850 and GSM900 frequency signal.

  - CM2=15pF (0402 package) for the TDMA noise coming from the demodulation of the DCS/PCS frequency signal.

These capacitors must be soldered in parallel to the microphone.

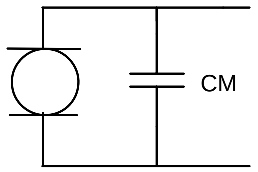


Figure 19: Microphone

5.8.2 Recommended Speaker Characteristics

- Type of speakers: Electro-magnetic /10mW
- Impedance: 32 to 150Ω.
- Sensitivity: 110dB SPL min
- Receiver frequency response compatible with the GSM specifications.

5.8.3 Recommended Filtering Components

When designing a GSM application, it is important to select the right audio filtering components.

The strongest noise, called TDMA, is mainly due to the demodulation of the GSM850/GSM900/DCS1800 and PCS1900 signal: A burst being produced every 4.615ms; the frequency of the TDMA signal is equal to 216.7Hz plus harmonics.

The TDMA noise may be suppressed by filtering the RF signal using the right decoupling components.

The types of filtering components are:

- RF decoupling inductors
- RF decoupling capacitors

A good Chip S-Parameter simulator is proposed by Murata, and the following link may help to find it:

http://www.murata.com/designlib/mcsil.html

Using different Murata components, it is observed that the value, the package and the current rating may have different decoupling effects.

The table below shows some examples with different Murata components:

Package	0402		
Filtered band	GSM900	GSM 850/900	DCS/PCS
Value	100nH	56pF	15pF
Types	Inductor	Capacitor	Capacitor
Position	Serial	Shunt	Shunt
Manufacturer	Murata	Murata	Murata
Rated	150mA	50V	50V
Reference	LQG15HSR10J02 or LQG15HNR10J02	GRM1555C1H560JZ01	GRM1555C1H150JZ01 or GRM1555C1H150JB01
Package	**0603**		
Filtered band	GSM900	GSM 850/900	DCS/PCS
Value	100nH	47pF	10pF
Types	Inductor	Capacitor	Capacitor
Position	Serial	Shunt	Shunt
Manufacturer	Murata	Murata	Murata
Rated	300mA	50V	50V
Reference	LQG18HNR10J00	GRM1885C1H470JA01 or GRM1885C1H470JB01	GRM1885C1H150JA01 or GQM1885C1H150JB01

5.8.4 Audio track and PCB Layout Recommendation

To avoid TDMA noise, it is recommended to surround the audio tracks by ground:

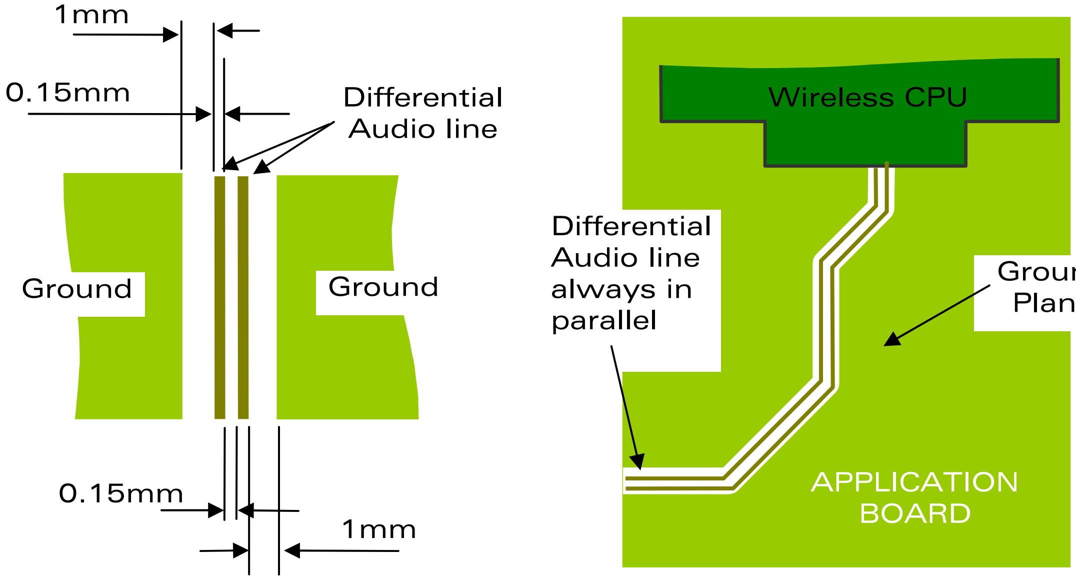


Figure 20: Audio track design

Note:

Avoid digital tracks crossing under and over the audio tracks.

5.8.5 Microphone Inputs

The MIC1 inputs do not include an internal bias. MIC1/SPK1 may be used either for a hands-free system or a handset with external biasing circuit for the microphone.

The MIC2 inputs already include the biasing for an electret microphone, allowing easy connection to a headset.

5.8.5.1 MIC1 Microphone Inputs

The MIC1 inputs are differential and do not include internal bias. To use these inputs with an electret microphone bias must be provided outside the Wireless CPU Q24 Series, according to the characteristic of this electret microphone.

These inputs are the standard inputs used for an external headset or a hands-free kit.

- Pin 42: MIC1P
- Pin 44: MIC1N

5.8.5.1.1 Typical Implementations

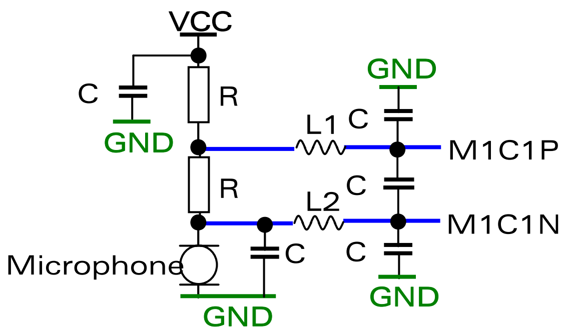
The microphone connections may be either differential or single-ended, but use of a differential connection in order to <u>reject common mode noise and TDMA noise is strongly recommended.</u>

<u>Single- ended connection</u>

<u>Caution:</u>

When using a single-ended connection, be sure to have a good ground plane, good filtering and also shielding, in order to avoid any disturbance on the audio path.

Typical implementation:



<u>PCB design advice:</u>

-The ground connection (in green) of each component of the audio MIC1 path should be common.
-The audio tracks MIC1P and MIC1N (in blue) should be routed in parallel and close together.
- It is better to surround the audio tracks completely with a ground

Figure 21: MIC1 inputs and single-ended connection

R1 = usually between 100 Ω to 330Ω, is used as a voltage supply filtered with C4 (47 µF Tantalum).

R2= usually between 1 kΩ and 3.3 kΩ as per the Vcc voltage level and the microphone characteristics.

C5 must be close to the microphone. Microphone manufacturers may provide this capacitor directly soldered on the microphone (see "Microphone recommendations").

L1, L2, C1, C2, and C3 are used to filter the TDMA noise. They must be as close as possible to the Wireless CPU connector.

The typical values may be (see the **RF filtering components recommendations for more information**):

C2 =C5=GSM RF filtering capacitors: used to filter the TDMA noise coming from the GSM band. This may be changed to DCS RF decoupling capacitors, if the TDMA noise comes from the DCS band.

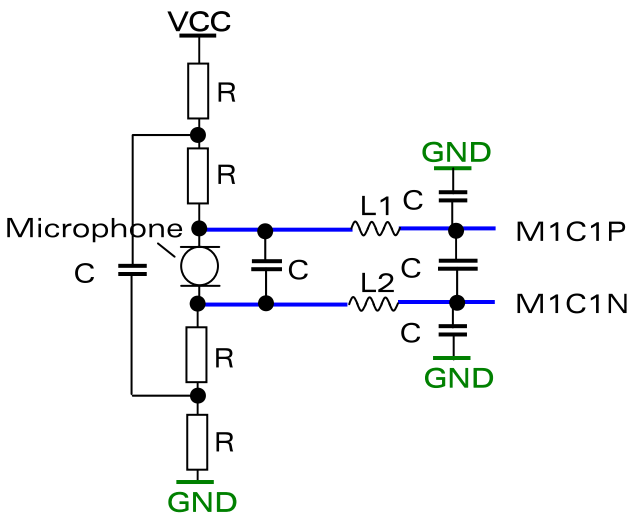
C1 = C3 = Not connected (package 0402), but have to be planned in case of TDMA noise.

L1 = L2 = GSM RF decoupling inductors.

Notes:

- To bias the microphone, it is mandatory to have a "**clean**" **VCC** signal.
- The VCC voltage may be the voltage provided from the Wireless CPU itself (Pin 40).
- TDMA noise depends mostly on the environment (grounding, shielding). TDMA noise may be determined once the final application is tested.
- According to the microphone characteristics and the surrounding environment, the component values may be tuned or removed in order to suppress the TDMA noise.

Differential connection



PCB design advice:

-The ground connection (in green) of each component of the audio MIC1 path should be common.
-The audio tracks MIC1P and MIC1N (in blue) should be routed in parallel and close together.
- It is better to surround the audio. tracks completely with a ground

Figure 22: MIC1 inputs and differential connection

R1=R4 = usually from 100Ω to 330Ω, are used as a voltage supply filter with C5 (47 µF Tantalum).

R2=R3 usually between 1 kΩ and 3.3 kΩ as per the VCC voltage level and the microphone characteristics.

C4 must be close to the microphone. Microphone manufacturers may provide this capacitor directly soldered on the microphone (see "Microphone recommendations").

L1, L2, C1, C2, and C3 are used to filter the TDMA noise. They must be as close as possible to the Wireless CPU connector.

The typical values may be (see the **RF filtering components recommendations** for more information):

C2 =C4= GSM RF filtering capacitors: Used to filter the TDMA noise coming from the GSM band. This may be changed to DCS RF decoupling capacitors if the TDMA noise comes from the DCS band.

C1 = C3=NC (package 0402), but have to be planned in case of TDMA noise.

L1 = L2 = GSM RF decoupling inductors.

Notes:

- To bias the microphone, it is mandatory to have a "clean" VCC signal.
- The VCC voltage may be the voltage provided from the Wireless CPU itself (Pin 40)
- The TDMA noise depends mostly on the environment (grounding, shielding)
- According to the microphone characteristics and the surrounding environment, the component values may be tuned or removed in order to suppress the TDMA noise.

5.8.5.2 MIC2 Microphone Inputs

The MIC2 inputs are differential inputs. They already include convenient biasing for an electret microphone (0.5 mA and 2 volts). This electret microphone may be directly connected to these inputs.

The impedance of microphone 2 must be around 2 kΩ. These inputs are the standard inputs for a handset design, while MIC1 inputs may be connected either to an external headset or a hands-free kit.

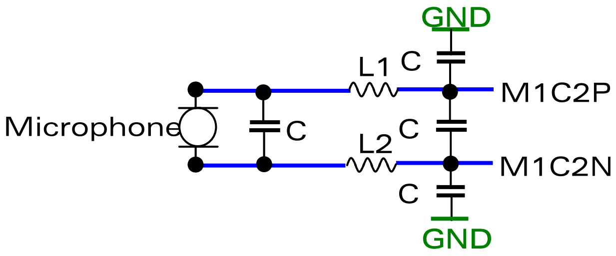
AC coupling is already embedded in the Wireless CPU:

- Pin 46: MIC2P
- Pin 48: MIC2N

5.8.5.2.1 Typical Implementations

The microphone connections may be either differential or single-ended, but using a differential connection in order to reject common mode noise and TDMA noise is strongly recommended.

5.8.5.2.2 Differential Connection



PCB design advice:

-The ground connection (in green) of each component of the audio MIC2 path should be common.
-The audio tracks MIC2P and MIC2N (in blue) should be routed in parallel and close together.
- It is better to surround the audio tracks completely with a ground

Figure 23: MIC2 inputs and differential connection

The components are mainly planned and used to filter the TDMA noise.

C4 must be close to the microphone. Microphone manufacturers may provide this capacitor directly soldered on the microphone (see "Microphone recommendations").

L1, L2, C1, C2, and C3 must be as close as possible to the Wireless CPU connector.

The typical values may be (see the **RF filtering components recommendations** for more information):

C2 =C4= GSM RF filtering capacitors: Used to filter the TDMA noise coming from the GSM band. This may be changed to DCS RF decoupling capacitors, if the TDMA noise comes from the DCS band.

C1 = C3=NC (package 0402), but have to be planned in case of TDMA noise.

L1 = L2 = GSM RF decoupling inductors.

Note:

- The TDMA noise depends mostly on the environment (grounding, shielding)
- According to the microphone characteristics and the surrounding environment, the component values may be tuned or removed, in order to suppress the TDMA noise.

5.8.5.3 Speaker Outputs

The Wireless CPU provides two identical speaker interfaces (SPK1 and SPK2).

Speaker outputs are push-pull amplifiers and may be loaded down to 150Ω and up to 1 nF.

The impedance of the speaker amplifier outputs in differential mode is: R ≤ 1 Ω +/-10 % .

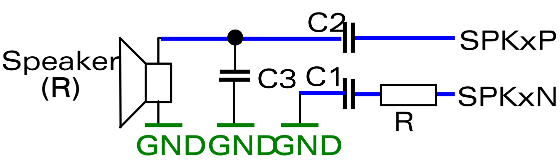
When speaker output is not used, the speaker interface is in three states and a 20K +/-30% impedance is kept between SPK1N and SPK1P as well as SPK2N and SPK2P.

- Pin 41: SPK1P
- Pin 43: SPK1N
- Pin 45: SPK2P
- Pin 47: SPK2N

5.8.5.3.1 Typical Implementations

The connection may be differential or single-ended, but using a differential connection to reject common mode noise and TDMA noise is strongly recommended. Moreover, in single-ended mode, the power is reduced by two compared to differential mode.

Single-ended connection



PCB design advice:

-The ground connection (in green) of each component of the audio SPKx path should be common.

-The audio tracks SPKxP and SPKxN (in blue) should be routed in parallel and close together.

- It is better to surround the audio tracks completely with a ground

Figure 24: Example of single-ended mode speaker implementation

C3=NC (package 0402), but must be planned and placed close to the speaker in case of TDMA noise.

In single-ended mode, it is necessary to add components in order to adapt the speaker to the output of the Wireless CPU speaker interface.

Typically: R1=impedance of the speaker (R)

R1&C1 and R&C2 are used to form two high pass filters, the recommended cut frequency of these filters is Fc=250 Hz.

These filters aim to attenuate the background and TDMA noise.

For a known Fc, the values of C1 and C2 are given by:

$$C1=C2=\frac{1}{2\Pi x R x Fc}$$

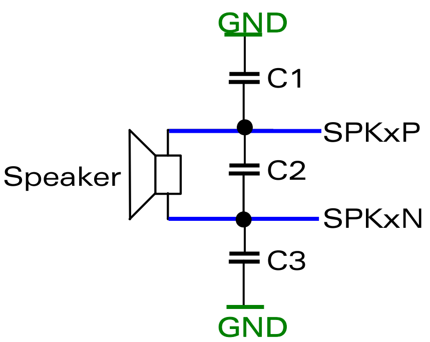
Examples	Speaker type	
R1 &R	32Ω	150Ω
C1 & C2	20µF (Tantalum or ceramic)	4.7µF (ceramic)

In case of a 32 Ω speaker, a cheaper solution may be used with R1=82 Ω and C1 =4.7 µF (ceramic).

Notes:

- TDMA noise depends mostly on the environment (grounding, shielding)
- According to the speaker characteristics and the surrounding environment, the component values may be tuned or removed in order to suppress the TDMA noise.

Differential connection



PCB design advice:

-The ground connection (in green) of each component of the audio SPKx path should be common.

-The audio tracks SPKxP and SPKxN (in blue) should be routed in parallel and close together.

- It is better to surround the audio tracks completely with a ground

The components are mainly planned and used to filter the TDMA noise.

C1 =C2=C3=NC (package 0402), but have to be planned and placed close to the speaker in case of TDMA noise.

Notes:

- TDMA noise depends mostly on the environment (grounding, shielding)
- According to the speaker characteristics and the surrounding environment, the component values may be tuned or removed in order to suppress the TDMA noise.

5.9 Buzzer Output

5.9.1 General Description

The buzzer interface is accessible through an open drain embedded on the Wireless CPU Q24 Series.

A buzzer may be directly connected between this output and VBATT.

- Pin 49: Buzzer (Buzzer output interface)

For further information on the Buzzer interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.9.2 Design Recommendation

The recommended characteristics of the buzzer are:

- Electro-magnetic type.
- Impedance: 7 to 30Ω.
- Sensitivity: 90 dB SPL min @ 10 cm.

Caution:

A diode against transient peak voltage must be connected as described below.

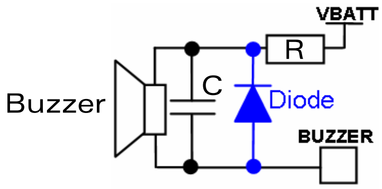


Figure 25: Buzzer connection

R: Used to limit the peak current in the buzzer (in general from 10Ω to 50Ω)
C: Used to filter the transient (in general from 0 to 100nF)

Note:

- The Wireless CPU accepts a maximum current of 100mA peak.

5.10 Battery Charging Interface

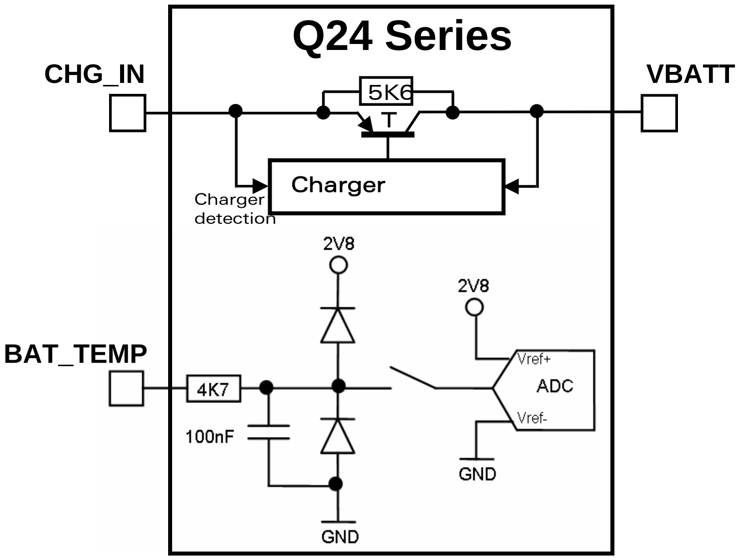
5.10.1 General Description

Caution:

- This interface does not allow the Wireless CPU to be supplied and is only used to charge a battery connected to VBATT.
- The battery charge starts if VBATT is higher than 2.8 volts.

Battery charging is performed through a switching transistor connecting the VBATT signal to the Charger (CHG_IN signal).

Equivalent circuit



- Pin 1,2,4 : CHG_IN (charger interface)
- Pin 38: BAT_TEMP (battery temperature monitoring)

The switching transistor is controlled by the operating system with different kinds of algorithms, depending on battery type.

The Wireless CPU Q24 Series supports three types of battery technologies:

- Ni-Cd (Nickel-Cadmium)
- Ni-Mh (Nickel-Metal Hydrure)
- Li-Ion (Lithium-Ion)

For further information on the battery charging interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.10.2 Design Recommendation

5.10.2.1 Charger Recommendation

The charger must be voltage and current limited.

This current value depends on the battery capacity. It is recommended to provide a current equal to the value of the capacity plus 50 mA.

Example:

For a 550 mA battery, the charger current may be 600 mA maximum.

Notes:

- The maximum acceptable voltage of the charger is 5.5 volts.
- The maximum acceptable charging current is 800 mA.

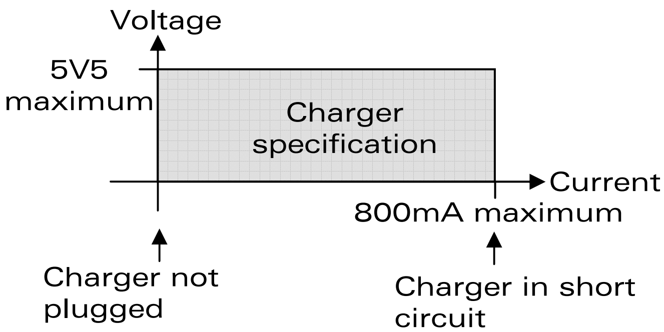


Figure 26: Charger recommendation

5.10.2.2 Battery Temperature Recommendation

Monitoring of the battery temperature of a Li-Ion battery is recommended for safety reasons.

A Li-Ion battery pack generally consists of:

- A cell (Energy Storage)
- A Protection Circuit Module (PCM) which aims to protect the battery pack against over-voltage mainly
- An NTC thermal resistor, where resistor value goes low when the temperature increases

For a Li-Ion battery, the Wireless CPU operating system allows battery temperature monitoring by connecting the BAT-TEMP to the NTC located in the battery pack:

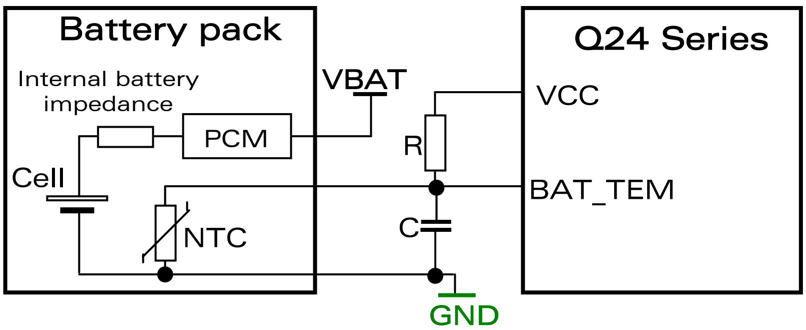


Figure 27: Example of battery implementation

To run properly, the operating system needs to know the minimum and maximum temperature acceptable by the battery pack. The temperatures may be set either by using an AT command or the Open AT API.

R and C selection:

- R must be selected to have a full range of BAT_TEMP (from 0V to 2V8) when the CTN value changes from the minimum to the maximum temperature.
- C must be selected to have a filter with a time constant lower than RxC=2 ms.

Examples:

Suppose a CTN with the following data:

$CTN_{(+25\ °C)} = 47\ k\Omega$

$CTN_{(+55\ °C)} = 10\ k\Omega$

$CTN_{(-10\ °C)} = 300\ k\Omega$

The value of R is given by the following formula:

$CTN_{(-10\ °C)} \times VCC = (CTN_{(-10\ °C)} + R) \times BAT\_TEMP_{(full\ range)}$

If VCC=2V8 and $BAT\_TEMP_{(full\ range)}$ =2V5 (for a good margin)

$R = 0.12 x CTN_{(-10\ °C)}$

$C_{max} = 2ms/R$

Then,

$R=40k\Omega$

In standard value, R= 47 kΩ

With C= 10 nF:

- RC(-10 °C) = 470 μs
- RC(+55 °C) = 100 μs

Hence,

$BAT\_TEMP_{(-10°C)} = 2V45$

$BAT\_TEMP_{(0°C)} = 1V4$

$BAT\_TEMP_{(+55\ °C)} = 0V5$

5.11 ON / ~OFF

5.11.1 General Description

- Pin 6: ON/OFF

This input is used to switch ON or OFF the Wireless CPU.

A high level signal must be provided on the ON/~OFF pin to switch ON the Wireless CPU.

The voltage level of this signal must be maintained between **2.4 V and 5V for a minimum of 1 s.**

This signal may be left at high level until switched OFF.

For further information on the ON/OFF interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification **[3]**.

5.11.2 Operating Sequences

5.11.2.1 Power-ON

Once the Wireless CPU is supplied by VBATT and VDD, the application must set the ON/~OFF signal to high to start the Wireless CPU power-ON sequence.

The ON/~OFF signal must be held for **1 sec minimum**. After this time, an internal mechanism maintains this on hold condition. During the power-ON sequence, the Wireless CPU for 240 ms (typical) automatically performs an internal reset. During this phase, any external reset should be avoided.

Once initialization is completed (timing is SIM and network dependent) the AT interface answers "OK" to the application[1]. For further details, please refer to the AT Commands documentation (AT+WIND, AT+WAIP).

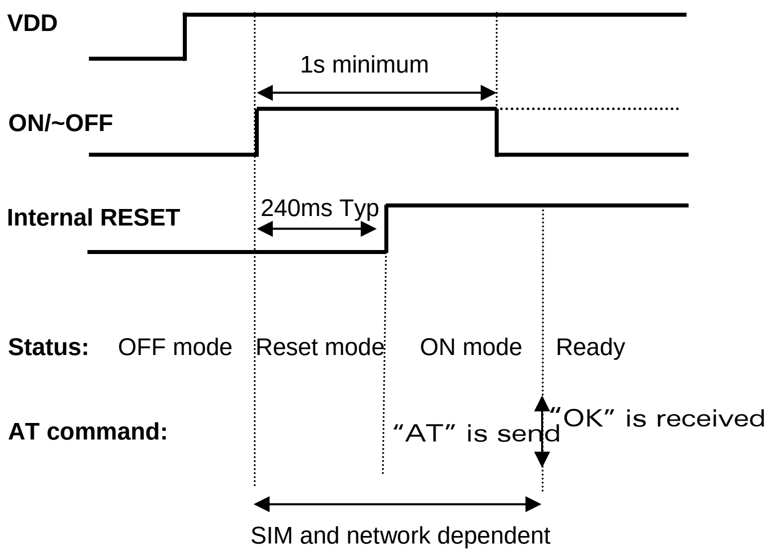


Figure 28: Power-ON sequence diagram

5.11.3.1 Power-OFF

To power-OFF the Wireless CPU correctly, the application must set the ON/~OFF signal to low and then send the AT+CPOF command to de-register from the network and switch off the Wireless CPU. Once the "OK" answer is issued, the Wireless CPU is set to OFF mode. Then the VDD and VBATT may be disconnected.

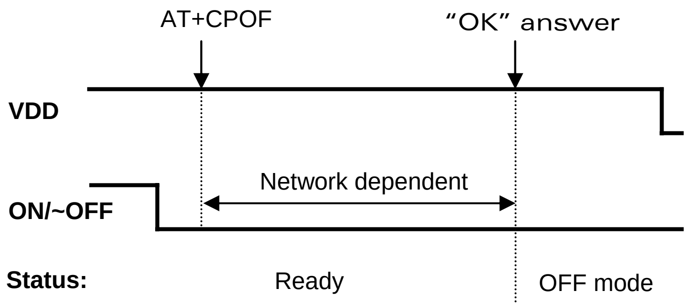


Figure 29: Power-OFF sequence diagram

Caution:

It is not allowed to power-OFF the Wireless CPU by disconnecting the supply pins VBATT and VDD.

5.12 BOOT (optional)

5.12.1 General Description

- Pin 12: BOOT

This input may be used to download software to the Flash memory of the Wireless CPU.

The internal BOOT procedure starts when this pin is low, during Wireless CPU reset.

For further information on the BOOT interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification[3].

Caution:

- This BOOT pin must be left open for normal use or Xmodem download.
- The nominal firmware download procedure uses the Xmodem.
- Even if this output is optional, for debug purposes, it is strongly recommended to implement an access to this pin in the application (test point, switch).

5.12.2 Design Recommendation

In Internal BOOT mode, low level must be set through a 1KΩ resistor.

- BOOT = logical state 0, for download mode and
- BOOT = logical state 1, for normal mode.

To drive the BOOT pin, it is possible either to use an open collector or an open drain output:

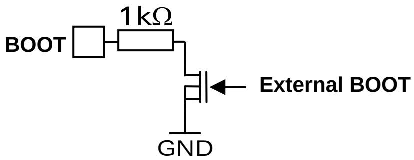


Figure 30: BOOT pin connection

5.13 Reset Signal (~RST)

5.13.1 General Description

- Pin 14: ~RST

The reset signal is used to force a reset procedure by providing low level, for at least 500 µs.

The Wireless CPU remains in reset mode as long as the ~RST signal is held low.

The reset process is activated either by the external ~RST signal or automatically by an internal signal (coming from a reset generator).

- ~RST = logical state 0, for Wireless CPU Reset and
- ~RST = logical state 1, for normal mode.

Notes:

A software reset is always preferred to a hardware reset.

The automatic reset is activated during a power-ON sequence.

During a power-ON sequence, the ~RST pin of the Wireless CPU is set to the logical state 0.

For further information on the Reset interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

Caution:

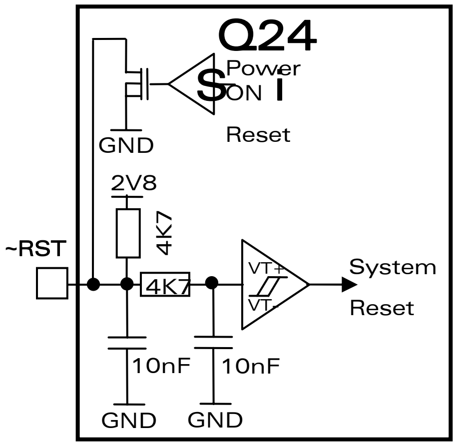
- During a power-ON sequence of the Wireless CPU, avoid applying any voltage to the ~RST pin.
- Otherwise:

  - The Wireless CPU reset procedure may not be correctly performed

- The Wireless CPU may be damaged

- Even if this output is optional, for debug purposes it is strongly recommended to implement an access to this pin in the application (test point, switch).

Equivalent circuit



This signal may also be used to provide a reset to an external device. It then behaves as an output. If no external reset is necessary, then this input may be left open.

5.13.2 Design Recommendation

If used (as emergency reset), an open collector or an open drain output must drive it:

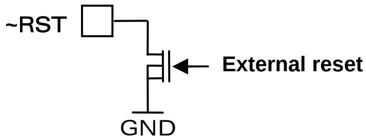


Figure 31: RST pin connection

To activate the "**emergency** "reset sequence, the ~RST signal must be set to low for **500 µs** minimum.

As soon as the reset is completed, the AT interface answers "**OK**" to the application.

In this case, the application must send AT↵. If the application manages hardware flow control, the AT commands may be sent during the initialization phase.

Another solution is to use the AT+WIND command to obtain an unsolicited status from the Wireless CPU.

For further details, refer to the AT Commands documentation [5].

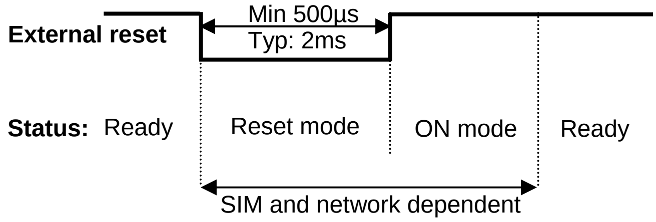


Figure 32: Reset sequence diagram

5.14 External Interrupt (~INTR)

5.14.1 General Description

- Pin 16: ~INTR

The Wireless CPU Q24 Series provide an external interrupt input ~INTR. This input is highly sensitive.

An interrupt is activated on a falling edge. If this signal is not used, it may be left open.

For further information on the Interrupt interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.14.2 Design Recommendation

If used, an open collector or an open drain output must drive it:

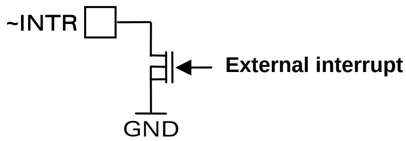


Figure 33: INTR pin connection

5.15 VCC Output

5.15.1 General Description

- Pin 40: VCC

This output is available to power some external functions. This power supply is available when the Wireless CPU is ON.

The maximum current, which may be provided, is 100mA.

For further information on the VCC interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.16 Real Time Clock Supply (VCC_RTC)

5.16.1 General Description

- Pin 56: VCC_RTC

The VCC_RTC input is used to provide a back-up power supply for the internal Real Time Clock (RTC).

If VDD<2.6V, the RTC regulator is disabled, a back-up battery is then necessary to save date and time information.

For further information on the VCC_RTC interface of the Wireless CPU Q24 Series, refer to the Product Technical Specification [3].

5.16.2 Design Recommendation

When the VDD pin of the Wireless CPU is not supplied or below 2V6, it mandatory to use a back-up battery or an external power supply connected to the VCC_RTC pin to save date and time information.

If the application does not require date and time information, this pin may be left open.

5.16.2.1 Back-up Battery Type

The types of back-up battery may be:

- Capacitor,
- Super capacitor,
- Non-rechargeable battery,
- Battery cell with regulator.

5.16.2.2 Typical Implementation

5.16.2.2.1 Capacitor or Super Capacitor

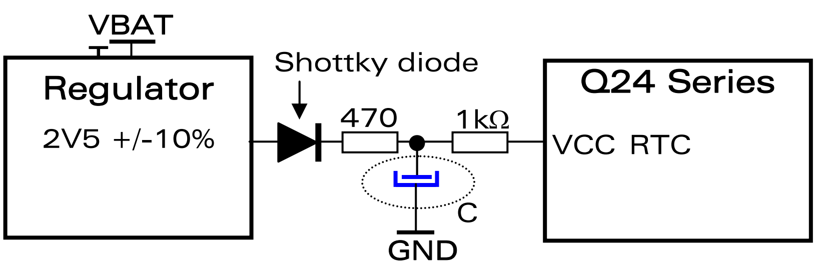


Figure 34: RTC Supplied by a capacitor or super capacitor

- Estimated range with C=470 μF capacitor: ~**30 seconds**.
- Estimated range with C=0.47 Farad gold super capacitor: **2 hours min**.

Note:

The reference for the gold super capacitor is an EECE0EL474S from Panasonic with a maximum voltage of 2V5.

5.16.2.2.2 Battery Cell with Regulator

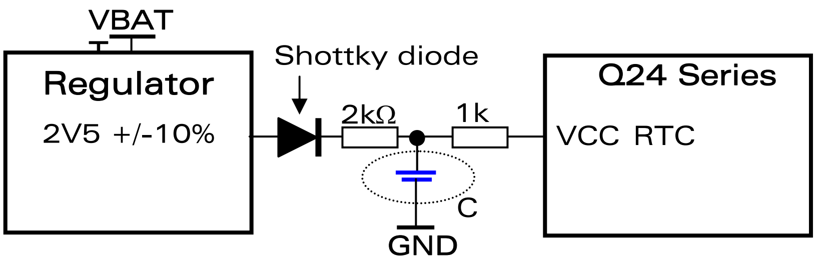


Figure 35: RTC Supplied by a battery cell

- Estimated range with 2 mAh rechargeable battery: ~**3 days**.

Before battery cell assembly, ensure that cell voltage is lower than 2.75V to avoid any damage to the Wireless CPU.

5.16.2.2.3 Non-Rechargeable Battery

This is the least recommended solution.

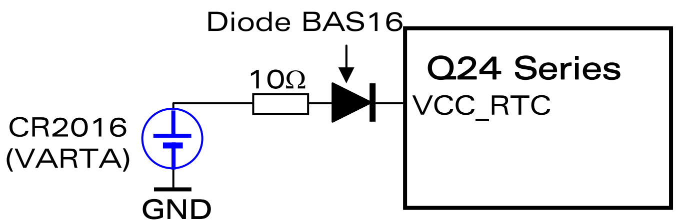


Figure 36: RTC supplied by a non-rechargeable battery

Estimated range with 85mAh battery: **4000 h minimum.**

Note:

The "non-rechargeable battery" is always active, except when the Wireless CPU is ON.

6 Radio Design

6.1 Antenna Characteristics Recommendation

The optimum operating frequency depends on the application. A dual-band or a quad-band antenna must operate in these frequency bands and have the following characteristics:

Characteristic		Q24 Series			
		EGSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50Ω			
VSWR	Rx max	1.5 :1			
	Tx max	1.5 :1			
Typical radiated gain		0dBi in one direction at least			

6.2 Antenna Implementation

The Wireless CPU impedance is 50 Ω nominal and the DC impedance is 0 Ω.

6.2.1 Recommendations

The antenna sub-system and its integration in the application are major issues.

Attention must be paid to the:

- Design of the antenna line on the application PCB,
- Antenna connector (type + losses),
- Antenna choice.

These elements may affect GSM performance factors such as sensitivity and emitted power.

The antenna should be isolated to the greatest extent possible from the digital circuitry (including the interface signals) ⇨ it is strongly recommended to shield the terminal.

On terminals including the antenna, a poor shielding could dramatically affect the sensitivity of the terminal. Moreover, the power emitted through the antenna may affect the application.

Wavecom strongly recommends working with an antenna manufacturer either to develop an antenna adapted to the application or to adapt an existing solution to the application. Antenna adaptation (mechanical and electrical adaptation) is one of the key issues in the design of a GSM terminal.

Caution:

- Avoid placing components around the RF connection and close to the RF line (between the module and the antenna).
- RF lines and cables must be as short as possible.
- The coaxial cable must not be placed close to devices operating at low frequencies.

6.2.2 RF connection

When the antenna is connected to the Wireless CPU through a 50 Ω coaxial cable, the coaxial cable must be connected to both the "Antenna pad" (or Round pad) and the "Ground pad" (see Figure 37).

It is recommended to use an RG178 coaxial cable with the following stripping and mounting guidelines:

- The antenna cable and connector must be selected in order to minimize losses in the frequency bands used for GSM 850/E-GSM 900MHz and DCS 1800/PCS 1900MHz.
- To obtain a good ground connection, the cable ground must be connected to the ground pad, as shown in Figure 37.

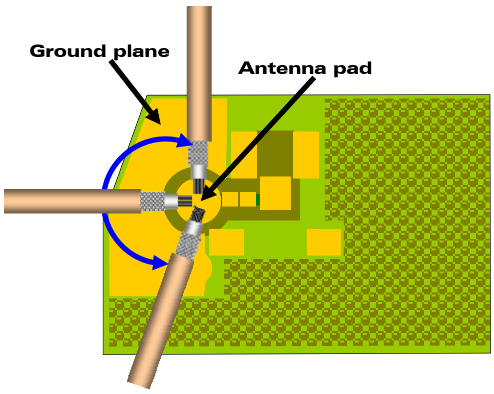


Figure 37: Antenna connection

Note:

For assembly of the RF cable on the Module, see the Wavecom recommendation for Manual Lead Free Soldering in section 13.1.

- Antenna cable preparation is shown in Figure 38.

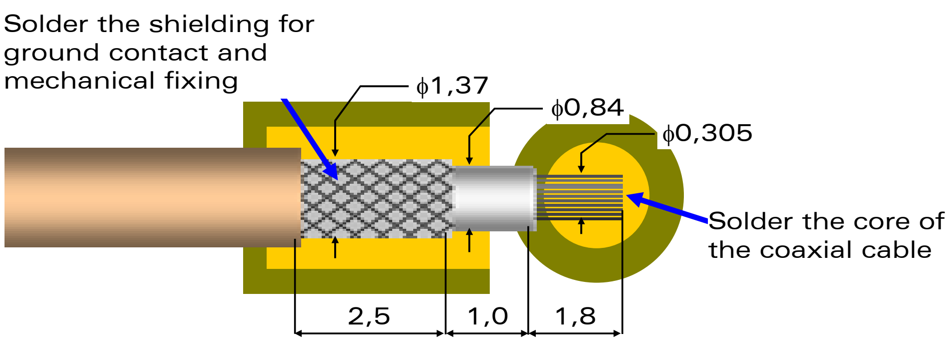


Figure 38: Antenna cable preparation

Notes:

- The Wireless CPU Q24 Series does not include any antenna switch for a car kit, but this function may be implemented externally and may be driven using a GPIO.
- 0.5 dB may be considered as a maximum value for loss between the Wireless CPU and an external connector.

7 ESD Immunity

Plastic enclosures, air space and insulation may prevent ESD arcs to equipment.

Ensure >= 5mm path length between the electronics and

- Any points that the user may touch, including seams, ventilation openings and mounting holes. At a given voltage, arcs may travel farther over the surface of a dielectric than they may through open air.
- Any ungrounded metal that the user may touch-fasteners, switches, control and indicators.
- Cover seams and mounting holes with Mylar tape inside the enclosure, extending past the edge of the seam/hole, to increase the path length, where clearance is limited.
- Cover unused or rarely used connectors with metal caps or insulating plastic dust covers.
- Use switches and controls with plastic shafts, or put plastic knobs or "tophats" on them, to increase the path length. Avoid knobs with metal setscrews.
- Recess LEDs and other indicators; cover them with tape or caps extending past the edge of the holes, or use light pipes to increase the path length.
- Extend the border on membrane keyboards >= 12mm outside the metal traces, or use a plastic bezel to increase the path length.
- Round the corners and edges on heat sinks and other metal parts that are close to seams, ventilating holes or mounting holes in the enclosure.
- Do not let metal fasteners protrude inside a plastic enclosure, if they will be anywhere close to the electronics or ungrounded metal.
- Put taller feet on a product to raise it off the table/floor, if the product fails indirect ESD tests to the table/floor or horizontal coupling plane.
- On tactile rubber keypads, keep the traces in tight and extend the rubber pieces to increase path length.
- Use adhesive/sealant around the circuitry layers of membrane keyboards.
- Use a high-voltage-proof silicone or poron gasket to provide an airtight, ESD-proof, waterproof, dustproof seal between pieces of the enclosure.

7.1 ESD Consideration

Circuit board layout is a critical design step in the suppression of ESD induced transients.

The following guidelines are recommended:

- The ESD diodes should be placed as close as possible to the input terminals or connectors.
- All conductive loops, including power and ground loops should be minimized.

- The ESD transient return path to ground should be kept as short as possible.
- Ground planes should be used whenever possible.
- A main precaution to take is to put the protection device closer to the disturbance source (generally the connector).
- The path length between the ESD suppressor and the protected line should be minimized:

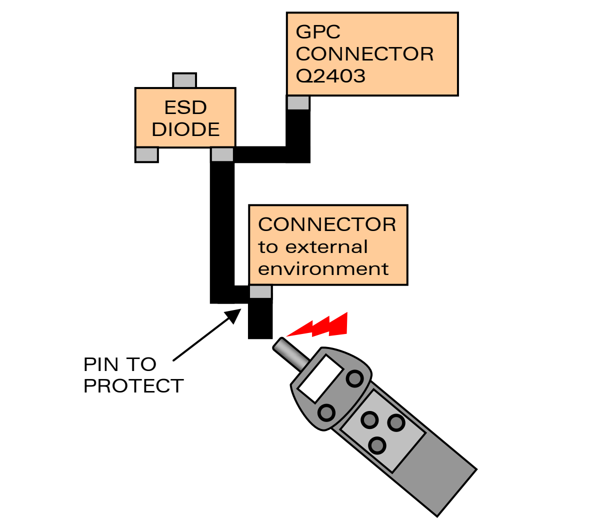


Figure 39: Shorter track to ESD Diode

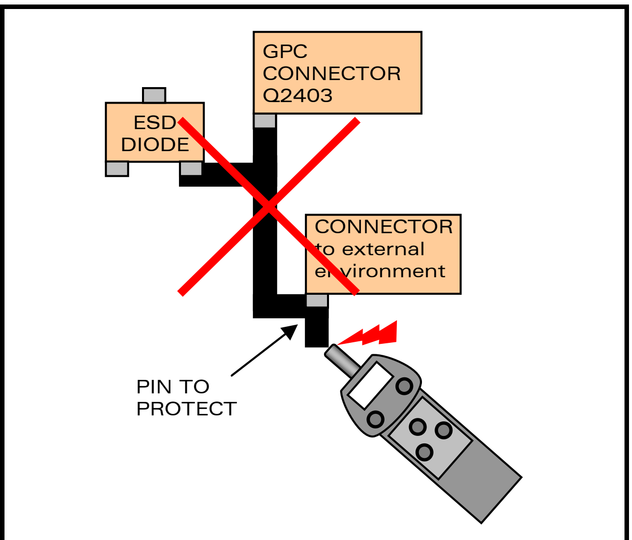


Figure 40: Configured way to avoid

7.2 PCB Layout against ESD

For a better ESD (Electrical Static Discharge) protection, good grounding planes should be presented around the PCB.

It is recommended to add ground planes on Top and Bottom layers as illustrated in the figure below. Best grounding may be achieved, if the planes and edges are connected by via holes.

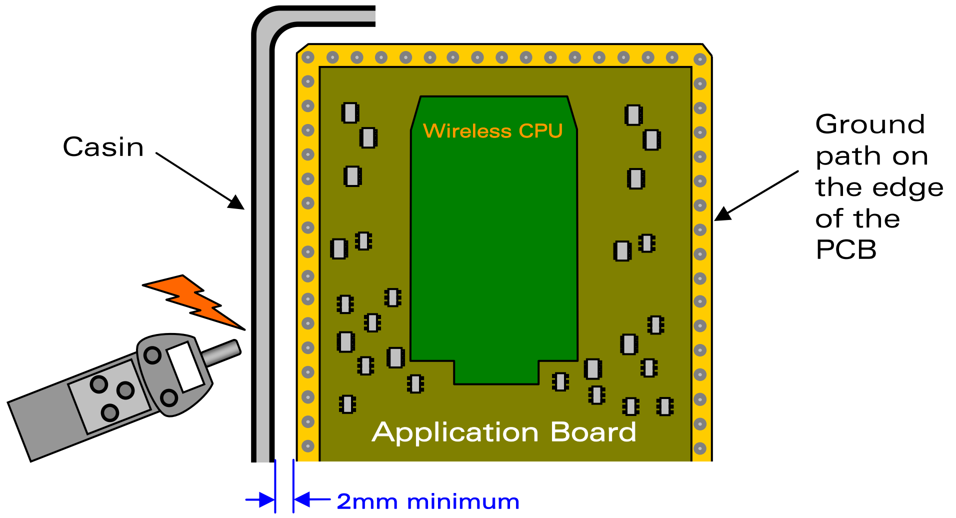


Figure 41: Top and Bottom Layers with ground plane

7.3 Stretch Cabinet Wall

For good isolation from the outside world, increasing the wall height is very important against ESD. There are two solutions to manufacture the front and rear cabinets. It is recommended to stretch the height of the inner wall.

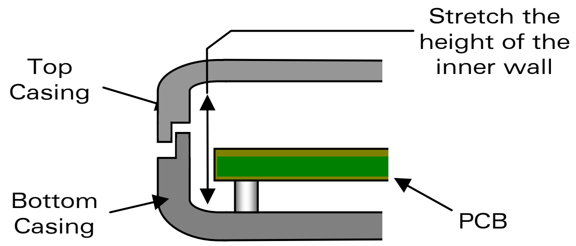


Figure 42: Stretch the height of the inner wall

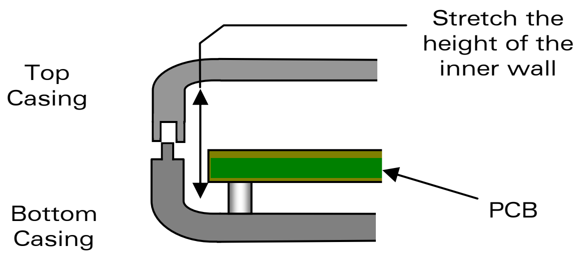


Figure 43: Stretch the height of the inner wall

8 EMC Recommendations

The EMC tests must be performed on the application as soon as possible to detect any problems.

- When designing, special attention should be paid to:
  - Possible spurious emissions radiated by the application to the RF receiver in the receiver band.
  - ESD protection on SIM (if accessible from outside), serial link, etc.
  - EMC protection on audio input/output (filters against 900 MHz emissions).

9 Technical Specifications

9.1 General Purpose Connector Pin-out Description

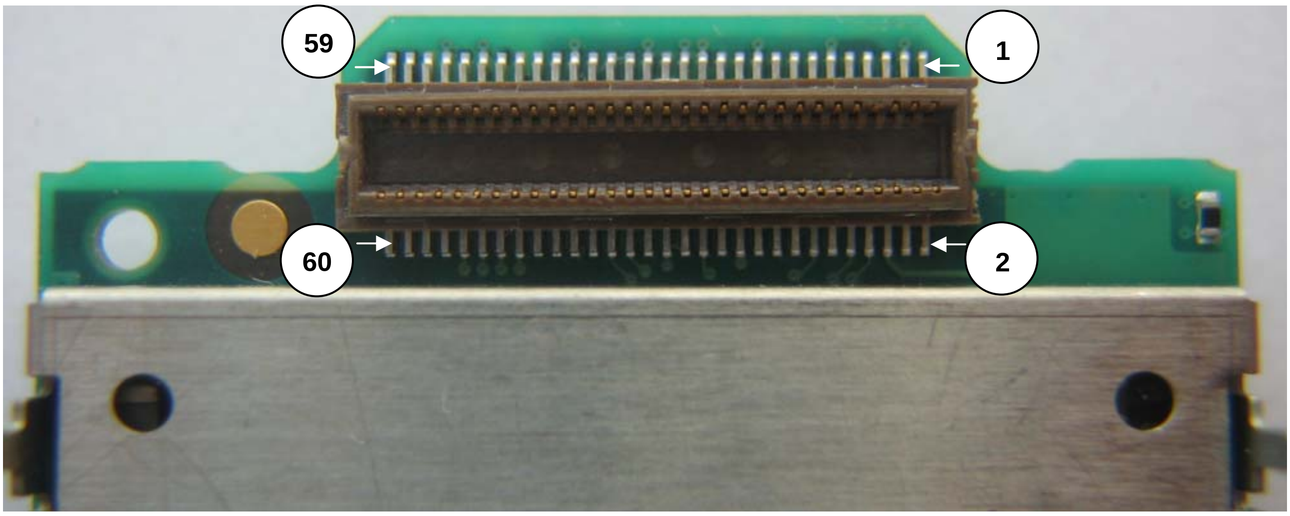


Figure 44: Wireless CPU pin position (bottom view)

Pin	Name	I/O	I/O type	Reset state	Description	Dealing with unused pins
1	CHG_IN	I	Supply	-	Supply for battery charging	Not connected
2	CHG_IN	I	Supply	-	Supply for battery charging	Not connected
3	SIM_CLK	O	-	0V	Clock for SIM interface	Not connected if Q24NG SIM CARD holder is used
4	CHG_IN	I	Supply	-	Supply for battery charging	Not connected
5	SIM_RST	O	-	0V	Reset for SIM interface	Not connected if Q24NG SIM CARD holder is used
6	ON/~OFF	I	CMOS	-	Power ON/OFF control	Must be used
7	SIM_DATA	I/O	-	0V	I/O for SIM interface	Not connected if Q24NG SIM CARD holder is used
8	SDA/SPI_IO	I/O	CMOS/CMOS 1X (C2)	Pull-up to 2V8	Two-wire interface or SPI Serial Data	Not connected

Pin	Name	I/O	I/O type	Reset state	Description	Dealing with unused pins
9	SIM_VCC	O	Supply	0V	SIM Card supply	Not connected if Q24NG SIM CARD holder is used
10	SCL/SPI_CLK	O	CMOS 1X (C5)	Pull-up to 2V8	Two-wire interface or SPI Serial clock	Not connected
11	VDD	I	Supply	-	Low power supply	Must be used
12	BOOT	I	CMOS (C5)	Pull-up to 2V8	BOOT	Test point (Download purposes)
13	ROW0	I/O	CMOS/ CMOS 1X	Pull-down	Keyboard Row	Not connected
14	~RST	I/O	Schmitt	0V	Reset	Test point (Debug purposes)
15	ROW1	I/O	CMOS/ CMOS 1X	Pull-down	Keyboard Row	Not connected
16	~INTR	I	CMOS (C5)	Pull-up to 2V8	External interrupt	Not connected
17	ROW2	I/O	CMOS/ CMOS 1X	Pull-down	Keyboard Row	Not connected
18	GPI or CT103/TXD2	I	CMOS (C4)	Pull-down to 0V	General Purpose Input or Transmit serial data (UART2)	Not connected
19	ROW3	I/O	CMOS/ CMOS 1X	Pull-down	Keyboard Row	Not connected
20	GPO2 or CT104/RXD2	O	CMOS 3X (C1) or CMOS 1X (C1)	2V8	General Purpose Output or Receive serial data (UART2)	Not connected
21	ROW4	I/O	CMOS/ CMOS 1X	Pull-down	Keyboard Row	Not connected
22	GPO1	O	CMOS 3X (C3)	0V	General Purpose Output	Not connected
23	COL0	I/O	CMOS/ CMOS 1X	Pull-up to 2V8	Keyboard Column	Not connected
24	GPIO0 or CT106/CTS2	I/O O	CMOS/CMOS 2X (C1) or CMOS 2X (C1)	High impedance	General Purpose I/O or Clear To Send (UART2)	Not connected
25	COL1	I/O	CMOS/ CMOS 1X	Pull-up to 2V8	Keyboard Column	Not connected
26	GPO0 or SPI_AUX	O O	CMOS 3X (C3) or CMOS 1X (C3)	2V8	General Purpose Output or SPI_AUX	Not connected
27	COL2	I/O	CMOS/ CMOS 1X	Pull-up to 2V8	Keyboard Column	Not connected

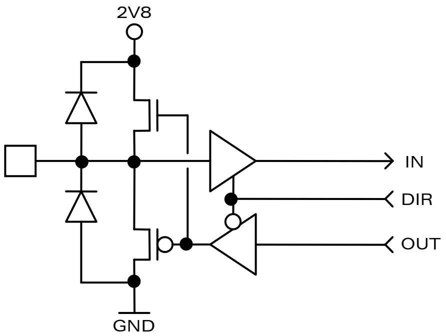
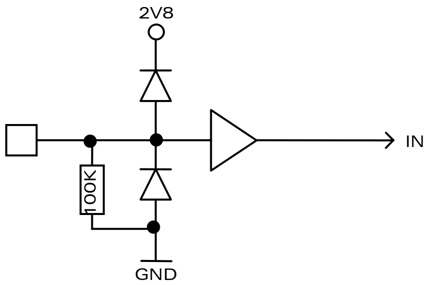
Pin	Name	I/O	I/O type	Reset state	Description	Dealing with unused pins
28	GPO3 or SPI_EN	O O	CMOS 3X (C3) or CMOS 1X (C3)	2V8	SPI enable or General Purpose Output	Not connected
29	COL3	I/O	CMOS/ CMOS 1X	Pull-up to 2V8	Keyboard Column	Not connected
30	CT105/RTS1	I	CMOS	High impedance	Request To Send (UART1)	100kΩ pull-up to 2V8 with test point (download and debug purposes)
31	COL4	I/O	CMOS/ CMOS 1X	Pull-up to 2V8	Keyboard Column	Not connected
32	CT104/RXD1	O	CMOS 1X (C3)	2V8	Receive serial data (UART1)	Test point (Download purposes)
33	AUXV0	I	Analog	High impedance	Auxiliary ADC input 0	Tied to GND
34	CT108-2/DTR1	I	CMOS	High impedance	Data Terminal Ready (UART1)	100kΩ pull-up to 2V8 with test point (download and debug purposes)
35	GPIO5 or CT105/RTS2	I/O I	CMOS/CMOS 2X (C1) or CMOS	High impedance	General Purpose I/O or Clear To Send (UART2)	Not connected
36	CT107/DSR1	O	CMOS 1X (C3)	2V8	Data Set Ready (UART1)	Not connected
37	CT106/CTS1	O	CMOS 1X (C1)	High impedance	Clear To Send (UART1)	Test point (Download purposes)
38	BAT_TEMP	I	Analog	High impedance	ADC input for battery temperature measurement	Tied to GND
39	CT103/TXD1	I	CMOS	High impedance	Transmit serial data (UART1)	100kΩ pull-up to 2V8 with test point (download and debug purposes)
40	VCC	O	Supply	2V8	2V8 digital supply output	Not connected
41	SPK1P	O	Analog	-	Speaker 1 positive output	Not connected
42	MIC1P	I	Analog	-	Microphone 1 positive input	Not connected
43	SPK1N	O	Analog	-	Speaker 1 negative output	Not connected

Pin	Name	I/O	I/O type	Reset state	Description	Dealing with unused pins
44	MIC1N	I	Analog	-	Microphone 1 negative input	Not connected
45	SPK2P	O	Analog	-	Speaker 2 positive output	Not connected
46	MIC2P	I	Analog	-	Microphone 2 positive input	Not connected
47	SPK2N	O	Analog	-	Speaker 2 negative output	Not connected
48	MIC2N	I	Analog	-	Microphone 2 negative input	Not connected
49	BUZZER	O	Analog	-	Buzzer output	Not connected
50	SIM_PRES	I	CMOS	High impedance	SIM Card Detect	Tied to 2V8
51	GPIO3 or CT109/DCD1	I/O O	CMOS/CMOS 2X (C1) or CMOS2X (C1)	High impedance	General Purpose I/O or Data Carrier Detect (UART1)	Not connected
52	GPIO1 FLASH LED	I/O O	CMOS/CMOS 2X (C1) or CMOS2X (C1)	High impedance	General Purpose I/O or Flash LED	Not connected
53	GPIO4	I/O	CMOS/CMOS 2X (C1)	High impedance	General Purpose I/O	Not connected
54	GPIO2 or CT125 / RI1	I/O O	CMOS/CMOS 2X (C1) or CMOS 2X (C1)	High impedance	General Purpose I/O or Ring Indicator (UART1)	Not connected
55	+VBATT	I	Supply	-	Battery Input	Must be used
56	VCC_RTC	I/O	Supply	2V8	RTC back-up supply	Not connected
57	+VBATT	I	Supply	-	Battery Input	Must be used
58	+VBATT	I	Supply	-	Battery Input	Must be used
59	+VBATT	I	Supply	-	Battery Input	Must be used
60	+VBATT	I	Supply	-	Battery Input	Must be used

9.2 I/O Circuit Diagram

The following drawings show the internal interface of the Wireless CPU Q24 Series.

The type indication per interface can be found in the previous chapters.

<table>
<tr><th>Type</th><th>Circuit</th><th>Type</th><th>Circuit</th></tr>
<tr><td>(C1)</td><td>
</td><td>(C4)</td><td>
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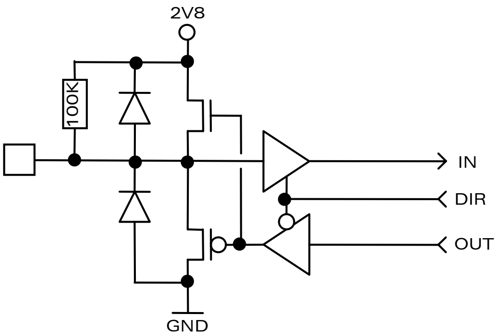
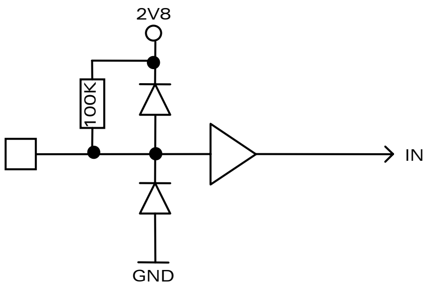
<tr><td>(C2)</td><td>
</td><td>(C5)</td><td>
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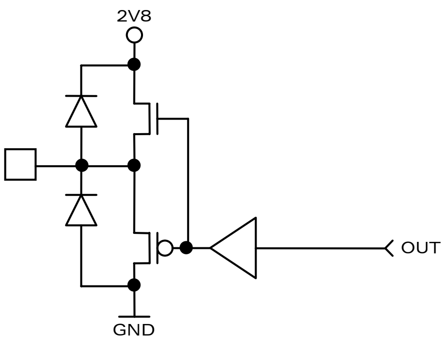
<tr><td>(C3)</td><td>
</td><td></td><td></td></tr>
</table>

10 PCB Layout in General

Clock and other high frequency digital signals (e.g parallel and serial buses) should be routed as far as possible from the Wireless CPU analog signals.

If the application design makes it possible, all analog signals should be separated from digital signals by a ground line on the PCB.

11 Debug and Testability

To easily debug an application, it is recommended to connect some signals directly to the General Purpose Connector of the application or to add some test points.

With a Wireless CPU, the sufficient signals needed to debug are:

1) RXD1, TXD1, RTS1, CTS1: for software traces
2) RXD2, TXD2, RTS2, CTS2: for software traces or to compute AT command when the UART1 is in data mode (Example: GPRS)
3) BOOT RESET: for download, purposes (also needs the signals required for software traces)
4) ON/OFF: to easily start the application
5) VBATT: to easily supply the Wireless CPU.

12 Firmware Upgrade

12.1 Recommendations

The Wireless CPU Q24 Series firmware is stored in flash memory and may easily be upgraded.

In order to keep with regular changes in the GPRS standard and to offer state-of-the-art software, Wavecom recommends that the application designed around a Wireless CPU Q24 Series allow easy firmware upgrades on the Wireless CPU via the standard Xmodem protocol.

Therefore, the application must either allow a direct access to the Wireless CPU serial link through an external connector or implement any mechanism allowing the firmware to be downloaded via Xmodem.

Caution:

The application must allow the Wireless CPU serial link signals, BOOT, RESET and the ON/~OFF signals of the Wireless CPU to be easily accessed, thus allowing the Wireless CPU firmware to be upgraded.

Two upgrade procedures are available:

1) Nominal upgrade procedure,
2) Backup procedure.

12.1.1 Nominal Upgrade Procedure

The firmware file may be downloaded into the modem using the Xmodem protocol.

To enter this mode, the AT+WDWL command (see the description in the AT command manual) must be sent.

The serial signals required to proceed with Xmodem downloading are:

RXD1, TXD1, RTS1, CTS1, and GND.

12.1.2 Backup Procedure

If nominal upgrade mode cannot be used (due to critical corruption on the flash memory), a backup procedure is also available. It requires specific software to download the firmware file into the Wireless CPU.

This tool must run on a PC connected to the serial bus of the modem.

The signals required to proceed with the downloading are RXD1, TXD1, RTS1, CTS1, and GND.

Prior to running the Wavecom downloader, the modem must be set to download mode.

To do this, the BOOT signal must be set to low, while powering-ON (or resetting) the Wireless CPU.

Tip: To reduce download time, serial link speed may be changed to 115200 bits/s. To do this, execute the AT command shown below:

1. AT+IPR=115200
2. AT+WDWL
3. file transfer
4. AT+CFUN=1 (reset of the module)

Caution:

After executing the last command (AT+CFUN=1), the speed of the serial link depends on the configuration of the binary file downloaded in the Wireless CPU.

13 Product Manufacturing Design Rules

Caution:

The Wireless CPU Q24 Series does not support any reflow soldering.

13.1 Recommendation for Lead Free Soldering

In order to maintain the RoHS status of the Wireless CPU, Wavecom recommends that *lead-free solder wire and flux* be used for Wireless CPU assembly on the motherboard and RF cable assembly on the Wireless CPU.

Example:

- Solder Wire: Kester 245 Cored 58 (Sn96.5Ag3Cu0.5)
- Flux: Kester 952-D6.

14 Mechanical Specifications

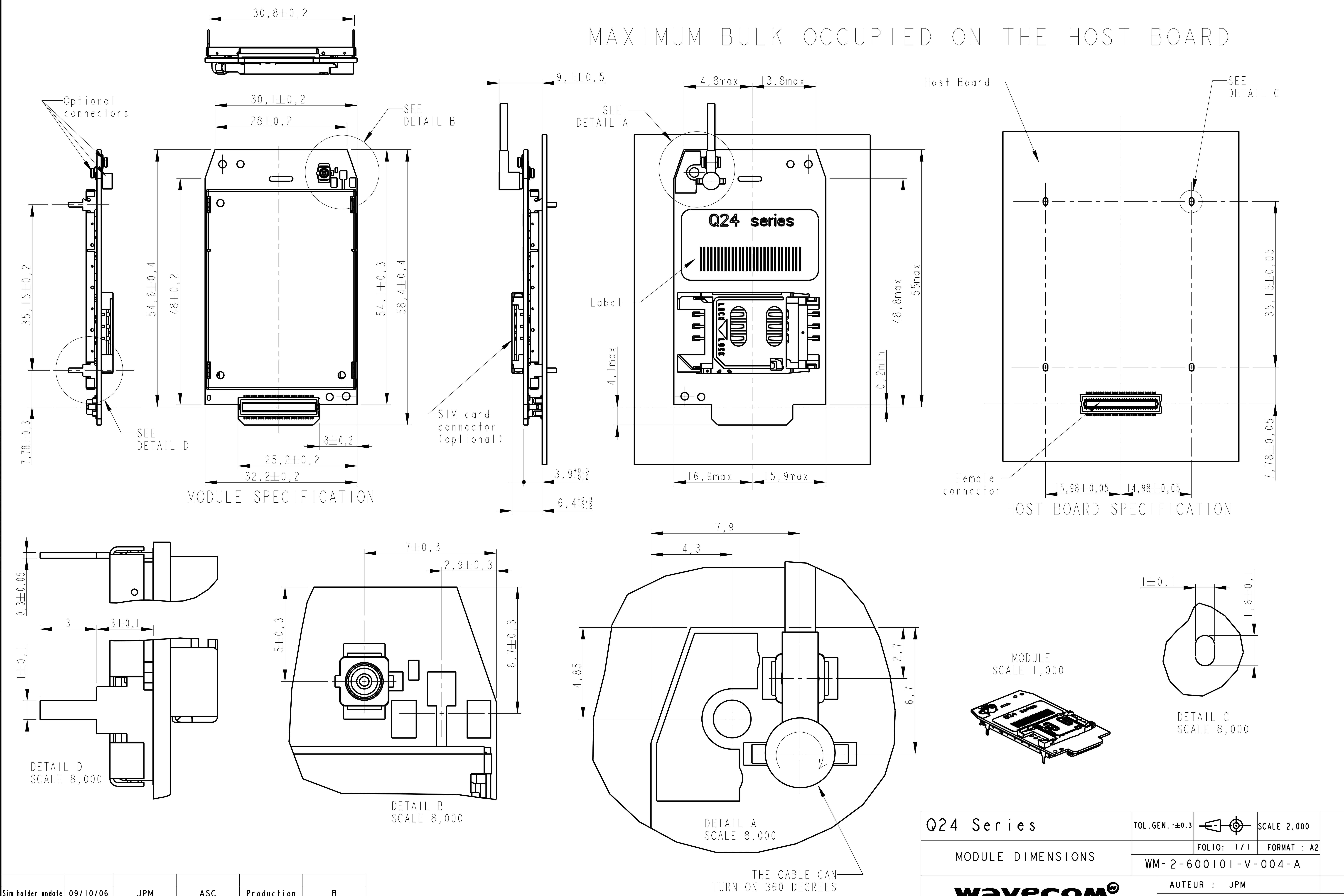
Attention should be paid to antenna cable integration (bending, length, position, etc).

Figure 45 gives the overall dimensions of the Wireless CPU, with PCB dimensions and placement tolerances taken into account.

It is important to assure that no component or mechanical element will enter into contact with the Wireless CPU, even in the event of vibration or manipulation of the final product.

These mechanical interferences may produce a bad electrical connection on the 60-pin General Purpose Connector.

Figure 45: Maximum area occupied on the application board (see next page)



Sim holder update	09/10/06	JPM	ASC	Production	B
Creation	03/08/06	JPM	ASC	Production	A
MODIFICATION	DATE	AUTHOR	RESP.	STATUS	IND

Q24 Series	TOL.GEN.:±0,3	SCALE 2,000
MODULE DIMENSIONS	FOLIO: 1/1	FORMAT : A2
	WM-2-600101-V-004-A	
wavecom	AUTEUR : JPM	
	RESPONS : ASC	B
PRO/ENGINEER Q24NG_ON_MB		IND.

14.1 Pad Design

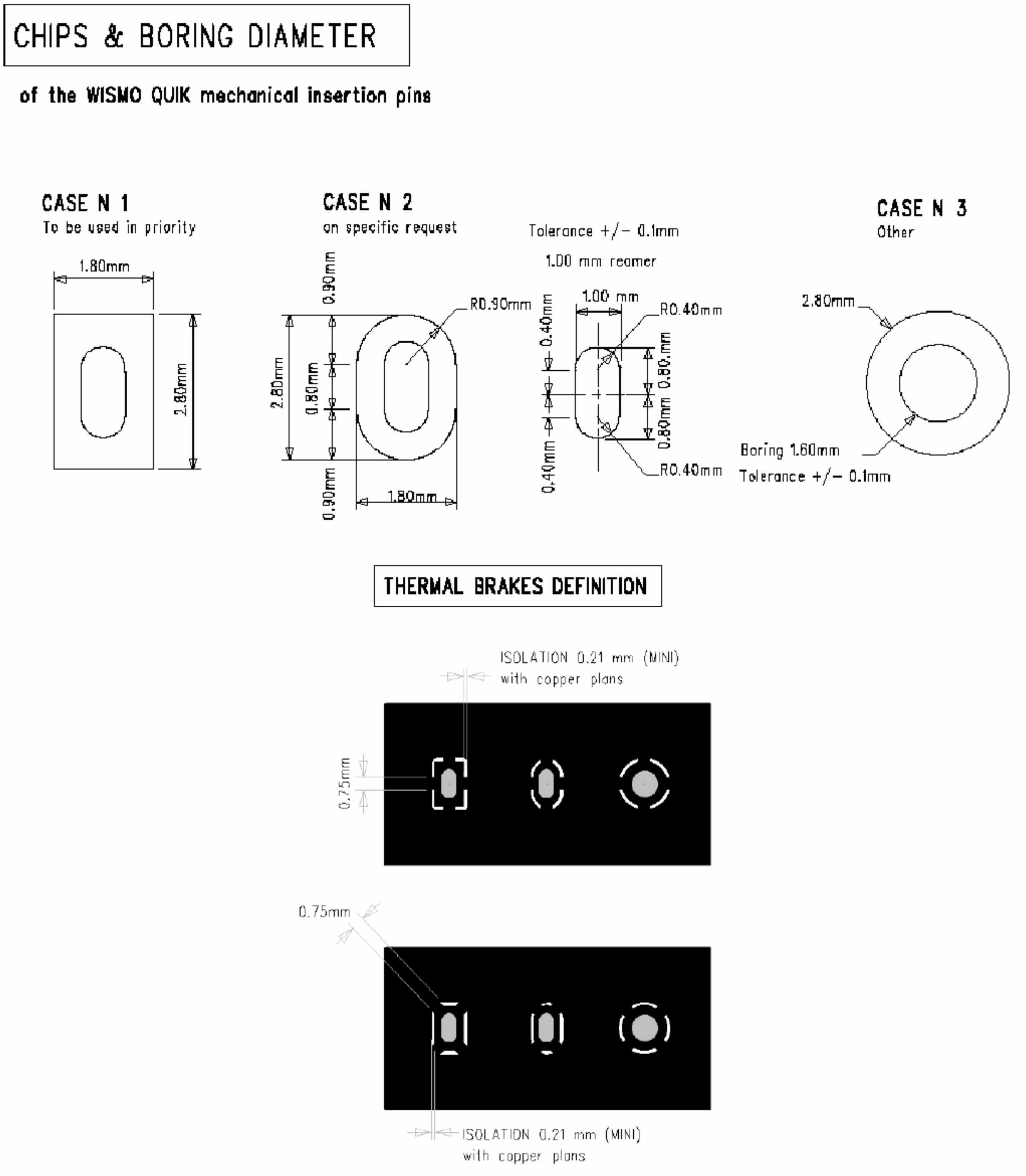


Figure 46: Pad design

14.2 Part References and Suppliers

14.3 General Purpose Connector

The GPC is a 60-pin connector with 0.5mm pitch from KYOCERA / AVX group with the following reference:

14 5087 060 930 861.

The matting connector has the following reference:

24 5087 060 X00 861, with X=2 or 9.

The stacking height is 3.0 mm.

For further details, see the GPC data sheets in the Appendix. More information is also available from http://www.avxcorp.com

14.4 SIM Card Reader

- ITT CANNON CCM03 series (see http://www.ittcannon.com)
- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.com)

Drawer type:

- MOLEX 99228-0002 (connector) / MOLEX 91236-0002 (holder) (see http://www.molex.com)

14.5 Microphone

Possible suppliers:

- HOSIDEN
- PANASONIC

14.6 Speaker

Possible suppliers:

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

14.7 Antenna Connections

14.7.1 Antenna Pad

The following cable reference has been qualified for mounting on antenna pads:

- RG178

14.7.2 IMP Connector (RF board to board)

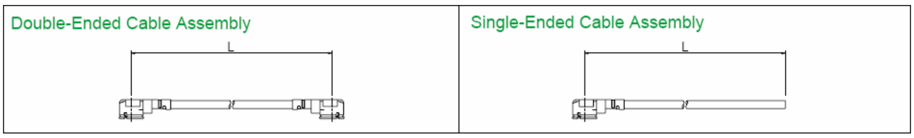
The supplier for the IMP connector is Radiall (http://www.radiall.com) with the following reference:

- R107 064 900 (or R107 064 902)

14.7.3 UFL Connector

A wide range of cables fitted with UF-L connectors is offered by HIROSE:

- UF-L pigtails
- UF-L cable assemblies
- Between series cable assemblies



, The following reference may be used for single-ended connectors:

- U.FL-LP-088K1T-A-(L) (L): Length to specify

More information is also available from:

http://www.hirose-connectors.com/products/U.FL_5.htm.

14.7.4 MMS Connector

The supplier for the MMS (ref: R209 408 302) connector is Radiall. More information is also available from:

http://www.radiall.com/vdocportal/portal/action/WebdriveActionEvent/oid/01g-00000c-02u

14.8 GSM Antenna

Provider	Reference	Address	Contact
Mat Equipement	MA112VX00	Z.I. La Boitardière Chemin du Roy 37400 Amboise FRANCE	Laurent.LeClainche@matequipement.com Tel: +33 2 47 30 69 70 Fax: +33 2 47 57 35 06
ProComm	MU 901/1801/UMTS-MMS + 2M FME	Europarc 121, Chemin des Bassins F-94035 CRETEIL CEDEX	Tel: +33 1 49 80 32 00 Fax: +33 1 49 80 12 54 procom@procom.fr

GSM antennas and support for antenna adaptation may be obtained from manufacturers such as:

- ALLGON (http://www.allgon.com)
- MOTECO (http://www.moteco.com)

Make it wireless

WAVECOM S.A. - 3 esplanade du Foncet - 92442 Issy-les-Moulineaux Cedex - France - Tel: +33(0)1 46 29 08 00 - Fax: +33(0)1 46 29 08 08
Wavecom, Inc. - 4810 Eastgate Mall - Second Floor - San Diego, CA 92121 - USA - Tel: +1 858 362 0101 - Fax: +1 858 558 5485
WAVECOM Asia Pacific Ltd. - Unit 201-207, 2nd Floor, Bio-Informatics Centre – No.2 Science Park West Avenue - Hong Kong Science Park, Shatin - New Territories, Hong Kong