Wireless CPU Q24NG
Product Technical Specification

Revision: **001**

Date: **May 2006**

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WIRELESS CPU Q24NG

Product Technical Specification

Reference: **WM_PRJ_Q24NG_PTS_001**
Revision: **001**
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Powered by the Wavecom Operating System and Open AT®

Document History

Revision	Date	History of the evolution	
001	May 2006	creation (Preliminary version)	

Overview

This document defines and specifies the Wireless CPU Q24NG., available in four different versions of GSM/GPRS Class 10 quad-band versions.

The Versions are described below:

- **Q24 Classic**: **EGSM 900/1800/850/1900** MHz version with **32** Mb of Flash memory and **16** Mb of PSRAM (**32/16**), T° range **[-20°C / +55°C]**.
- **Q24 Plus**: **EGSM/GPRS 900/1800/850/1900** MHz version with **32** Mb of Flash memory and **16** Mb of PSRAM (**32/16**), T° range **[-20°C / +55°C]**.
- **Q24 Extended**: **EGSM/GPRS 900/1800/850/1900** MHz version with **32** Mb of Flash memory and **4** Mb of SRAM (**32/4**), T° range **[-40°C / +85°C].**
- **Q24 Automotive**: **EGSM/GPRS 900/1800/850/1900** MHz version with **32** Mb of Flash memory and **4** Mb of PSRAM (**32/4**), T° range **[-40°C / +85°C]**.

This version is dedicated to the automotive applications.

Contents

Table of figures

Cautions

This platform contains a modular transmitter. This device is used for wireless applications. Note that all electronics parts and elements are ESD sensitive.

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1 References

1.1 Reference documents

For more details, several reference documents may be consulted. The Wavecom reference documents are provided in the Wavecom document package contrary to the general reference documents which are not Wavecom owned.

1.1.1 Wavecom reference documents

[1] Automotive Environmental Control Plan for Wireless CPU Q24NG
WM_PRJ_Q24NG_DCP_001

[2] Environmental Control Plan for Wireless CPU Q24NG
WM_PRJ_Q24NG_DCP_002

[3] Wireless CPU Q24NG Customer Design Guidelines
WM_PRJ_Q24NG_PTS_002

[4] Wireless CPU Q24NG Process Customer Guidelines
WM_PRJ_Q24NG_PTS_003

[5] AT Commands Interface Guide for OS 6.57
TBD

1.1.2 General reference documents

[6] "I²C Bus Specification", Version 2.0, Philips Semiconductor 1998

[7] ISO 7816-3 Standard

1.2 Abbreviations

Abbreviation	Description
3GPP	Third Generation Partnership Project
ADC	Analog to Digital Converter
A/D	Analog to Digital conversion
AT	ATtention (prefix for modem commands)
AUX	AUXiliary
CBS	Cell Broadcast Service
CLK	CLocK
CMOS	Complementary Metal Oxide Semiconductor
CODEC	CODer DECoder
CPU	Central Processing Unit
CTS	Clear To Send
dB	Decibel
DC	Direct Current
DCD	Data Carrier Detect
DCS	Digital Cellular System
DCXO	Digitally controlled crystal oscillator
DR	Dynamic Range
DSR	Data Set Ready
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EGSM	Extended GSM
EN	ENable
ESD	ElectroStatic Discharges
ETSI	European Telecommunications Standards Institute
FEM	Front End Module
FR	Full Rate
GND	GrouND
GPI	General Purpose Input
GPC	General Purpose Connector
GPIO	General Purpose Input Output
GPO	General Purpose Output
GPRS	General Packet Radio Service
GSM	Global System for Mobile communications

Abbreviation	Description
IF	Intermediate Frequency
INTR	INTeRrupt
I/O	Input / Output
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LSB	Less Significant Bit
MAX	MAXimum
MIC	MICrophone
MIN	MINimum
MMS	Multimedia Message Service
MS	Mobile Station
NOM	NOMinal
NTC	Negative Temperature Coefficient
PA	Power Amplifier
PBB	PolyBrominated Biphenyl
PBDE	PolyBrominated Diphenyl Ethers
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communications Services
PLL	Phase Lock Loop
RAM	Random Access Memory
RF	Radio Frequency
RI	Ring Indicator
RoHS	Restriction of Hazardous Substances
RST	ReSeT
RTC	Real Time Clock
RTS	Request To Send
RX	Receive
SCL	Serial CLock
SDA	Serial DAta
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPK	SPeaKer

Abbreviation	Description
SRAM	Static RAM
TDMA	Time Division Multiple Access
TU	Typical Urban fading profile
TUHigh	Typical Urban, High speed fading profile
TDMA	Time Division Multiple Access
TX	Transmit
TYP	TYPical
UART	Universal Asynchronous Receiver-Transmitter
VLSI	Very Large Scale Integration
VSWR	Voltage Standing Wave Ratio

2 General description

2.1 General information

The Wireless CPU Q24NG is a self-contained EGSM/GPRS 900/1800 and 850/1900 quad-band Wireless CPU with the following characteristics :

2.1.1 Overall dimensions

- Length: 58.4 mm
- Width: 32.2 mm
- Thickness: 3.9 mm (6,2 mm for Q24 Automotive which offers on MMS or UFL connector on the top side)

2.1.2 Environment and mechanics

- Green policy: RoHS compliant
- Complete shielding

The Q24NG Wireless CPU is compliant with RoHS (Restriction of Hazardous Substances in Electrical and Electronic Equipment). Directive 2002/95/EC which sets limits for the use of certain restricted hazardous substances. This directive states that "from 1st July 2006, new electrical and electronic equipment put on the market does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE)".

Wireless CPUs which are compliant with this directive are identified by the RoHs logo on their label.

2.1.3 GSM/GPRS Features

- 2 Watts EGSM 900/GSM 850 radio section running under 3.6 Volts
- 1 Watt GSM1800/1900 radio section running under 3.6 Volts
- Hardware GPRS class 10 capable

2.1.4 Interfaces

- Digital section running under 2.8 Volts.
- Optional SIM holder.
- Complete interfacing is through a 60-pin connectors. It includes:
  - 3V/1.8V SIM interface
  - Power supply
  - Serial link
  - Audio
  - SIM card interface
  - Keyboard
  - LCD

2.1.5 Operating system

- Real Time Clock with calendar
- Battery charger
- Echo Cancellation and noise reduction (quadri codec)
- Full GSM or GSM/GPRS Operating System stacks

2.1.6 Connection interfaces

The Q24NG is offered with different external connection configurations:

- Q24 Classic, Q24 Plus and Q24 Extended
  - Three for RF circuit:
    - UFL connector (bottom side)
    - Soldered connection (top side)
    - IMP connection (bottom side)
  - One for base band signals:

60 pin I/O connector (bottom side).

- Q24 Automotive
  - Two for RF circuit
    - UFL or MMS connector (top side)
    - Soldered connection (top side)
  - One for base band signals:
    - 60 pin I/O connector (bottom side)

2.2 Functional description

The global architecture of Q24NG is described below:

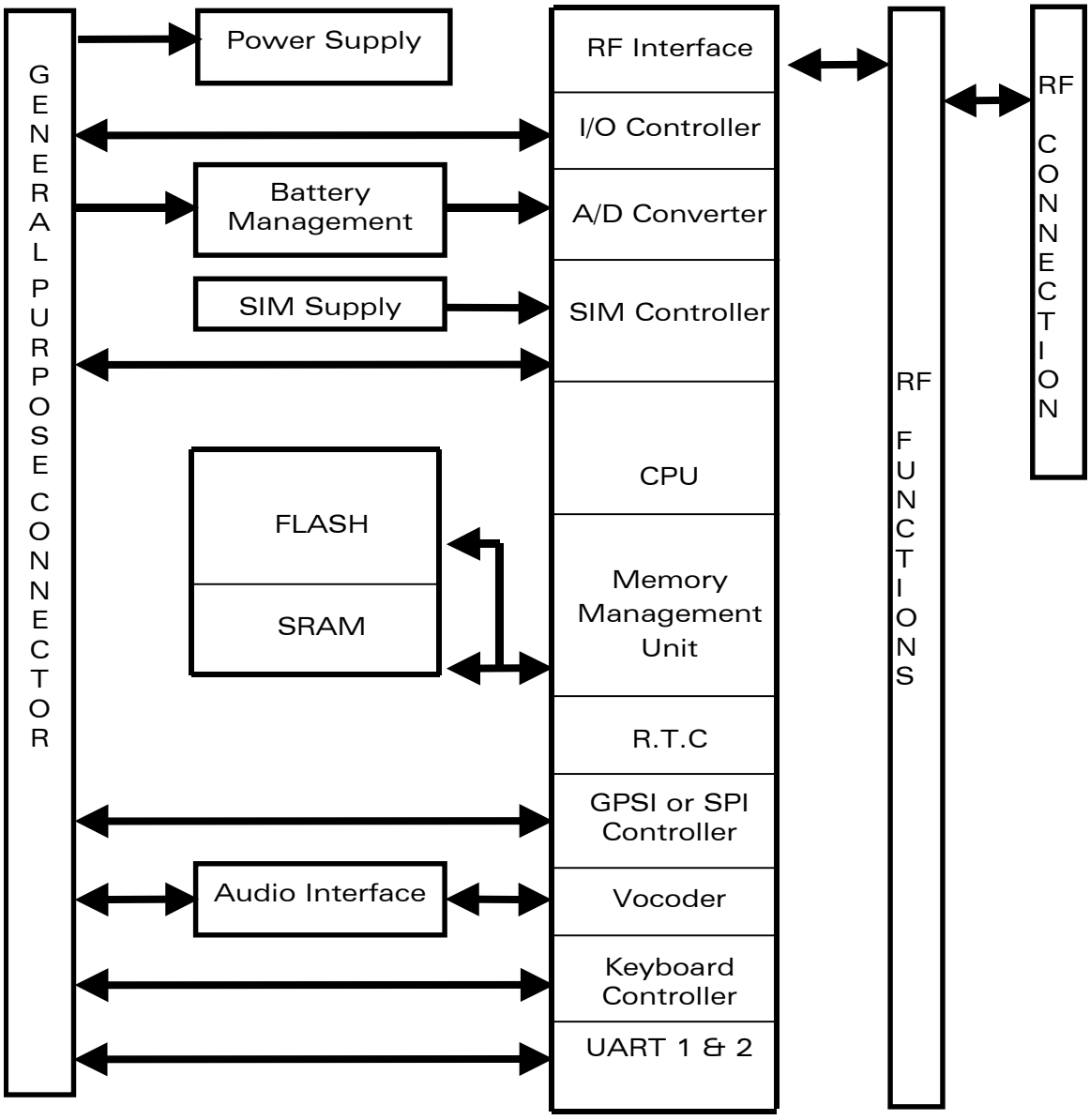


Figure 1: Functional architecture

2.2.1 RF functionalities

The Radio Frequency (RF) range comply with the Phase II EGSM 900/DCS 1800 and GSM 850/PCS 1900 recommendation. The frequencies are given below:

	Transmit band (Tx)	Receive band (Rx)
GSM 850	824 to 849 MHz	869 to 894 MHz
EGSM 900	880 to 915 MHz	925 to 960 MHz
DCS 1800	1710 to 1785 MHz	1805 to 1880 MHz
PCS 1900	1850 to 1910 MHz	1930 to 1990 MHz

The Radio Frequency (RF) part is based on a specific quad band chip. It includes:

- a Digital low-IF receiver,
- a Quad-band LNAs (Low Noise Amplifier),
- an Offset PLL (Phase Locked Loop) transmitter,
- a Frequency synthesizer,
- a Digitally controlled crystal oscillator (DCXO),
- a Tx/Rx FEM (Front-End Wireless CPU) for quad-band GSM/GPRS.

2.2.2 Baseband functionalities

The digital part of the Q24NG is based on the PHILIPS-VLSI chip (ONE C GSM / GPRS Kernel).

This chipset uses a 0.25 µm CMOS mixed technology, which allows massive integration as well as low current consumption.

2.3 Operating System

The Q24NG is designed to integrate various types of specific process applications such as vertical applications (telemetry, multimedia, automotive...).

The Operating System offers a set of AT commands to control the Wireless CPU. With this standard Operating System, some interfaces of the Wireless CPU are not available since they are dependent on the peripheral devices connected to the Wireless CPU.

This symbol is used to indicate that the interfaces are not available with AT commands.

The Operating System is Open AT® compliant.

3 Interfaces

Note:

Some of the Wireless CPU Q24NG interface signals are multiplexed in order to limit the total number of pins. But this architecture implies some limitations.

Example: Instead of using the SPI bus, the 2-wire bus cannot be used.

Caution:

All external signals must be inactive when the Q24NG Wireless CPU is OFF. This is to avoid any damage while starting and to allow the Q24NG Wireless CPU to start correctly.

3.1 General Purpose Connector (GPC)

A 60-pin connector, with 0.5 mm pitch, is provided to interface the Wireless CPU Q24NG sub-series with a board containing either an LCD Wireless CPU, or a keyboard, or a SIM connector, or a battery connection, etc..

The GPC is made by the KYOCERA / AVX group with the following reference:

- 14 5087 060 930 861.

The matting connector has the following reference:

- 24 5087 060 X00 861.

For further details, refer to section 5.1General Purpose Connector data sheet.

The available interfaces on the GPC are described below.

Section	Name	Driven by OS 6.57	Not driven by OS 6.57	Driven by Open AT®	Not driven by Open AT®
3.4	Serial interfaces	X		X	
3.5	Keyboard Interface	X		X	
3.6	Main Serial Link	X		X	
3.7	Auxiliary Serial Link	X		X	
3.8	SIM Interface	X		X	
3.9	General Purpose IO	X		X	
3.11	Analog to Digital Converter	X		X	
3.12	Audio Interface	X		X	
3.13	Battery Charging Interface	X		X	
3.14	ON OFF	X		X	
3.15	Boot		X		X
3.16	Reset	X		X	
3.17	External Interrupt	X		X	
3.18	VCC Output	X		X	
3.19	Real Time Clock supply	X		X	

3.2 Power supply

3.2.1 Power supply description

The power supply is one of the key issue in the design of a GSM terminal.

Due to the burst emission in GSM / GPRS, the power supply must be able to deliver high current peaks in a short time. During these peaks the ripple (Uripp) on the supply voltage must not exceed the limits specified in the table "Maximum voltage ripple (Uripp) vs Frequency" below.

- In communication mode, a GSM/GPRS class 2 terminal emits 577µs radio bursts every 4.615ms. (See Figure 2: Power supply during burst emission).
- In communication mode, a GPRS class 10 terminal emits 1154µs radio bursts every 4.615ms.

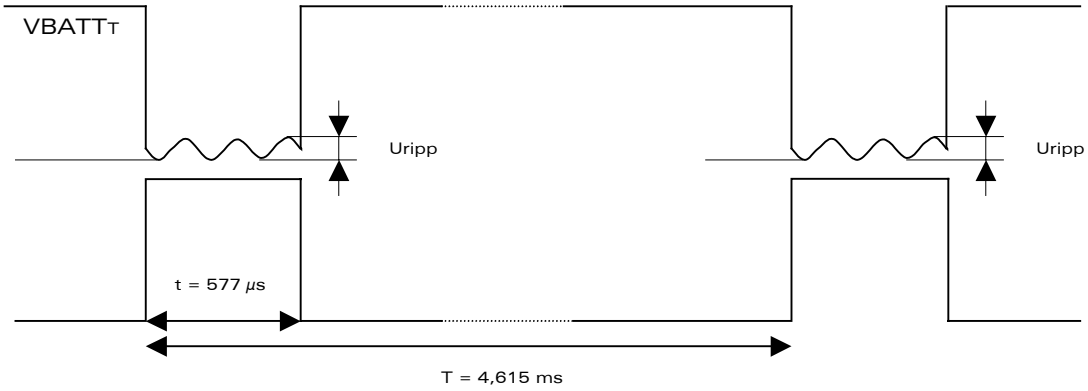


Figure 2: Power supply during burst emission

Two different inputs are provided for the power supply:

- the first one, VBATT, is used to supply the RF part,
- the second one, VDD, is used to supply the baseband part.

Notes:

- It is possible to connect VBATT to VDD.
- In case of separate power supplies, they must be in the same state ie both active or inactive at the same time.

VBATT: directly supplies the RF components with 3.6 V. It is essential to keep a minimum voltage ripple at this connection in order to avoid any phase error. The RF Power Amplifier current (2.0 A peak in GSM /GPRS mode) with a 50Ω RF output flows with a ratio of:

- 1/8 of the time (around 577 µs every 4.615 ms for GSM/GPRS class 2),
- 2/8 of the time (around 1154 µs every 4.615 ms for GSM/GPRS class 10).

The rise time is around 10 µs.

VDD: supplies the +2.8 V ballast regulators of the WISMO Wireless CPU. It is essential to keep the voltage over 3.1 volts.

The Wireless CPU Q24NG shielding case is the grounding. The ground has to be connected to the mother board through a complete layer on the PCB.

The power supply voltage for VBATT and VDD is given below:

	Vmin	Vnom	Vmax
VBATT	3.2 V *	3.6 V	4.5 V **
VDD	3.1 V		4.5 V

* This value has to be guaranteed during the burst (with 2.0 A Peak in GSM or GPRS mode).

** max operating Voltage Standing Wave Ratio (VSWR) 2:1.

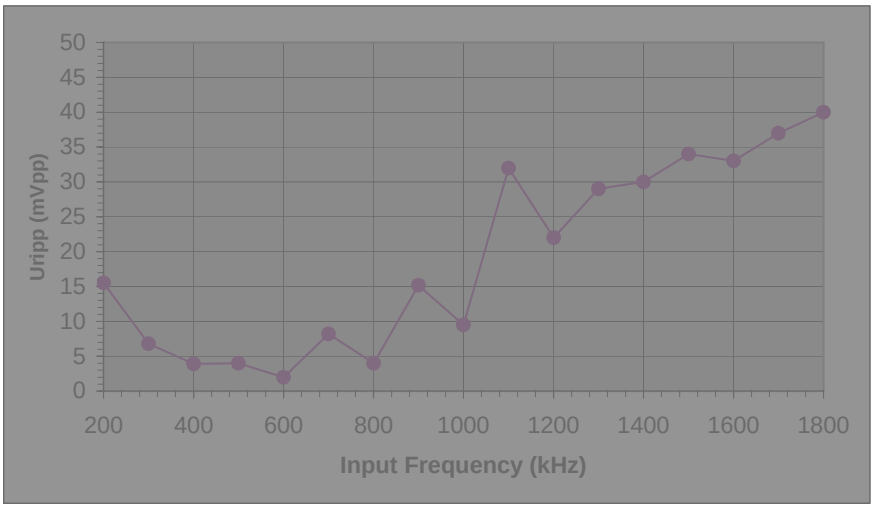
When the Wireless CPU is supplied with a battery, the total impedance (battery + contacts + protections + PCB) should be < 150MΩ to limit voltage drop-out within emission burst.

As the radio power amplifier is directly connected to the VBATT, the Wireless CPU is sensitive to any Alternating Current on lines. When a DC/DC converter is used, Wavecom recommends to set the converter frequency in such a way that the resulting voltage does not exceed the values. The values are given in the following table.

Maximum voltage ripple (Uripp) vs Frequency

Freq. (kHz)	U_{ripp} Max (mVpp)	Freq. (kHz)	U_{ripp} Max (mVpp)	Freq. (kHz)	U_{ripp} Max (mVpp)
<100	50	800	4	1500	34
200	15.5	900	15.2	1600	33
300	6.8	1000	9.5	1700	37
400	3.9	1100	32	1800	40
500	4	1200	22	>1900	40
600	2	1300	29		
700	8.2	1400	30		

To be confirmed



for f<100kHz U_{ripp} Max = 50mVpp
for f> 1800kHz U_{ripp} Max = 40 mVpp

Figure 3: Maximal voltage ripple (Uripp) vs Frequency in GSM & DCS

Refer to the Wireless CPU Q24NG Customer Design Guidelines [3] for further information about power supply design.

3.2.2 Power consumption

The power consumption depends on the configuration used. It is for this reason that the following consumption values are given for each modes, RF bands and software used (AT or Open AT®).

All the following information is given assuming a 50 Ω RF output.

The consumption values are given by measurement on Wireless CPU sampling. Three VBATT values are used to measure the consumption, $VBATT_{MIN}$ (3.2V), $VBATT_{MAX}$ (4.5V) and $VBATT_{TYP}$ (3.6V).

The average current is given for the three VBATT values and the peak current given is the maximum current peak measured with the three VBATT voltages.

For more information about consumption measurement, hardware configuration, SIM used, and software Dhrystone application, see AT Command Interface Guide or OS 6.57 [5] and Wireless CPU Q24NG Customer Design Guidelines [3].

When the Wireless CPU is in Alarm mode, no voltage must be applied to any pin of the 60-pin connector except on the BAT-RTC (pin 56) for RTC operation or ON/~OFF (pin 6) to power ON the Wireless CPU.

3.2.2.1 Power consumption

The following information is given assuming a 50 Ω RF output.

Power consumption in OFF mode
(Wireless CPU supplied, OFF state, no software running)

	Conditions	I_{NOM}	I_{MAX}
Overall consumption VBATT + VDD	Off	5 µA	10 µA

Power consumption in EGSM/GPRS 900 MHz and GSM/GPRS 850 MHz mode class 10

	Conditions	I_{NOM}	I_{MAX}
VBATT+VDD	During TX bursts @PCL5	1.60 A peak	1.8 A peak
	During RX bursts	110 mA peak	115 mA peak
	Average 1Rx/1Tx @PCL5	250 mA	300 mA
	Average 1Rx/1Tx @PCL8	190 mA	200 mA
	Average GPRS Cl 10 (3Rx/2Tx) @PCL5	400 mA	510 mA
	Average GPRS Cl 10 (3Rx/2Tx) @PCL8	260 mA	300 mA
	Average Idle mode	3 mA	7 mA

Power Control Level: PCL5=2 W typ.; PCL8=0.5 W typ.

Power consumption in GSM/GPRS 1800 MHz and GSM/GPRS 1900 MHz mode class 10

	Conditions	INOM	IMAX
VBATT+VDD	During TX bursts @PCL0	1 A peak	1.5 A peak
	During RX bursts	130 mA peak	140 mA peak
	Average 1Rx/1Tx @PCL0	190 mA	235 mA
	Average 1Rx/1Tx @PCL3	150 mA	180 mA
	Average GPRS Cl 10 (3Rx/2Tx) @PCL0	320 mA	410 mA
	Average GPRS Cl 10 (3Rx/2Tx) @PCL3	240 mA	270 mA
	Average Idle mode	2 mA	6.5 mA

Power Control Level: PCL0=1 W typ ; PCL3=0.25 W typ.

3.2.2.2 Power supply pinout

Power Supply Pinout

Signal	Pin number
VBATT	55,57; 58; 59; 60
VDD	11
GND	Shielding

The grounding connection is made through the shielding, the four legs have to be soldered to the ground plane.

3.3 Electrical information for digital I/O

All digital I/O comply with 3 Volts CMOS.

Operating conditions

Parameter	I/O type	Min	Max	Condition
VIL	CMOS	-0.5 V	0.8 V	
VIH	CMOS	2.1 V	3.0 V	
VOL	1X		0.2 V	IOL = -1 mA
	2X		0.2 V	IOL = -2 mA
	3X		0.2 V	IOL = -3 mA
VOH	1X	2.6 V		IOH = 1 mA
	2X	2.6 V		IOH = 2 mA
	3X	2.6 V		IOH = 3 mA

3.4 Serial interfaces

3.4.1 SPI bus

The SPI bus includes a CLK signal (SPI_CLK), an I/O signal (SPI_IO) and an EN signal (SPI_EN) complying with the SPI bus standard.

Pin description

Signal	Pin number	I/O	I/O type	Description
SPI_CLK	10	O	1X	SPI Serial Clock
SPI_IO	8	I/O	CMOS / 1X	SPI Data
SPI_EN *	28	O	1X	SPI Enable

* Multiplexed with GPO3.

3.4.2 Two-wire interface

The two-wire interface includes a CLK signal (SCL) and a DATA signal (SDA) complying with a standard 96 kbits/s interface. The maximum transfer speed is 400 kbits/s.

Note:

The two-wire interface is reserved for future use. A software emulated version of this interface using GPIOs is available. See the "AT Command Interface Guide" [5] for more information.

Pin description

Signal	Pin number	I/O	I/O type	Description
SCL	10	O	1X	Serial Clock
SDA	8	I/O	CMOS / 1X	Serial Data

3.4.3 SPI Auxiliary bus

A second SPI Chip Enable (called SPI_AUX) has to be used to add an SPI peripheral to the Wireless CPU Q24NG sub-series.

Pin description

Signal	Pin number	I/O	I/O type	Description
SPI_CLK	10	O	1X	SPI Serial Clock
SPI_IO	8	I/O	CMOS / 1X	SPI Data
SPI_AUX *	26	O	1X	SPI Aux. Enable

* Multiplexed with GPO0.

3.5 Keyboard interface

Caution:

This interface is not FULLY available with AT commands:

An AT command allows the input key code to be obtained (see the AT+CMER command description). This code must then be processed by the application.

This interface provides 10 connections:

- 5 rows (ROW0 to ROW4)
- 5 columns (COL0 to COL4)

The scanning is digital, and the debouncing is performed in the Wireless CPU. No discrete components such as R, C (Resistor, Capacitor) are needed.

Pin description

Signal	Pin number	I/O	I/O type	Description
ROW0	13	I/O	CMOS / 1X	Row scan
ROW1	15	I/O	CMOS / 1X	Row scan
ROW2	17	I/O	CMOS / 1X	Row scan
ROW3	19	I/O	CMOS / 1X	Row scan
ROW4	21	I/O	CMOS / 1X	Row scan
COL0	23	I/O	CMOS / 1X	Column scan
COL1	25	I/O	CMOS / 1X	Column scan
COL2	27	I/O	CMOS / 1X	Column scan
COL3	29	I/O	CMOS / 1X	Column scan
COL4	31	I/O	CMOS / 1X	Column scan

3.6 Main serial link (UART1)

A flexible 6-wire serial interface is available complying with V24 protocol signaling but not with V28 (electrical interface) due to a 2.8 Volt interface.

The signals are:

- TX data (CT103/TX)
- RX data (CT104/RX)
- Request To Send (CT105/RTS)
- Clear To Send (CT106/CTS)
- Data Terminal Ready (CT108-2/DTR)
- Data Set Ready (CT107/DSR)

The set of serial link signals may be required for GSM DATA services applications and is generated by the general purpose I/O provided by the Wireless CPU Q24NG.

The two additional signals are:

- Data Carrier Detect (CT109/DCD).
- Ring Indicator (CT125/RI).

Pin description

Signal	Pin number	I/O	I/O type	Description
CT103/TXD1	39	I	CMOS	Transmit serial data
CT104/RXD1	32	O	1X	Receive serial data
CT105/RTS1	30	I	CMOS	Request To Send
CT106/CTS1	37	O	1X	Clear To Send
CT107/DSR1	36	O	1X	Data Set Ready
CT108-2/DTR1	34	I	CMOS	Data Terminal Ready
CT109/DCD1 *	51	O	CMOS / 2X	Data Carrier Detect
CT125/RI1 **	54	O	CMOS / 2X	Ring Indicator
CT102/GND	Shielding legs			Ground

* Multiplexed with GPIO3

** Multiplexed with GPIO2.

The rising time and falling time of the reception signals (mainly CT103) have to be less than 200 ns.

The Wireless CPU Q24NG sub-series has been designed to be operated using all the serial interface signals. In particular, it is necessary to use RTS and CTS signals for hardware flow control in order to avoid data corruption during transmission.

3.7 Auxiliary serial link (UART2)

For current applications (e.g. Bluetooth connectivity) an auxiliary serial interface (UART2) will be available on the Wireless CPU Q24NG sub series.

Pin description

Signal	Pin number	I/O	I/O type	Description	Multiplexed with
CT103 / TXD2	18	I	CMOS	Transmit serial data	GPI
CT104 / RXD2	20	O	3X	Receive serial data	GPO2
CT106 / CTS2	24	O	2X	Clear To Send	GPIO0
CT105 / RTS2	35	I	CMOS	Request To Send	GPIO5

3.8 SIM interface

3.8.1 General Description

The following five signals are available:

- SIM_VCC: SIM power supply.
- SIM_RST: reset.
- SIM_CLK: clock.
- SIM_DATA: I/O port.
- SIM_PRES: SIM card detect.

The SIM interface controls a 3V / 1V8 SIM (and a 5V SIM through an external SIM driver). This interface is fully compliant with the GSM 11.11 recommendations concerning SIM functions.

Pin description

Signal	Pin number	I/O	I/O type	Description
SIM_CLK	3	O	2V9/1V8	SIM Clock
SIM_RST	5	O	2V9/1V8	SIM Reset
SIM_DATA	7	I/O	2V9/1V8	SIM Data
SIM_VCC	9	O	2V9/1V8	SIM Power Supply
SIM_PRES	50	I	2V8	SIM Card Detect

Electrical Characteristics

Parameter	Conditions	Min	Type	Max	Unit
SIM_DATA VIH	I_{IH} = ± 20 µA	0.7xSIMVCC			V
SIM_DATA VIL	I_{IL} = 1 mA			0.3xSIMVCC	V
SIM_RST, SIM_CLK VOH	Source current = 20 µA	0.9xSIMVCC			V
SIM_DATA	Source current = 20 µA	0.8xSIMVCC			V
SIM_RST, SIM_DATA SIM_CLK VOL	Sink current = -200 µA			0.4	V
SIM_VCC* Output Voltage	SIMVCC = 2.9V	2.84	2.90	2.96	V
	SIMVCC = 1.8V	1.77	1.8	1.86	V
SIM_CLK Rise/Fall Time	Loaded with 30 pF		20		ns
SIM_RST, Rise/Fall Time	Loaded with 30 pF		20		ns
SIM_DATA, Rise/Fall Time	Loaded with 30 pF		0.7		µs
SIM_CLK Frequency	Loaded with 30 pF			3.25	MHz

Note for SIM_PRES connection:

- When not used, SIM_PRES has to be tied to 1V8
- When used, a low to high transition means that the SIM card is inserted and a high to low transition means that the SIM card is removed.

3.8.2 SIM Holder

An optional SIM holder can be placed on top of the Wireless CPU.

When a SIM holder is used, through additional ESD components located close to the SIM holder, the Wireless CPU Q24NG is itself protected against electrostatic discharge.

3.9 General Purpose Input/Output

The Wireless CPU Q24NG sub-series provides:

- 6 General Purpose I/O,
- 4 General Purpose Outputs,
- 1 General Purpose Input.

They are used to control any external device such as an LCD or a Keyboard backlight.

Pin description

Signal	Pin number	I/O	I/O type	Description	Multiplexed with
GPIO0	24	I/O	CMOS / 2X	General Purpose I/O	CT106/CTS2
GPIO4	53	I/O	CMOS / 2X	General Purpose I/O	
GPIO5	35	I/O	CMOS / 2X	General Purpose I/O	CT105/RTS2
GPO0	26	O	3X	General Purpose O	SPI_AUX
GPO1	22	O	3X	General Purpose O	
GPO2	20	O	1X	General Purpose O	CT104/RXD2
GPI	18	I	CMOS	General Purpose I	CT103/TXD2
GPO3	28	O	CMOS	General Purpose O	SPI_EN

The following GPIOs are not available (reserved) with a Wireless CPU running with the AT commands firmware:

Signal	Pin number	I/O	I/O type	Description	Multiplexed with
GPIO1	52	I/O	CMOS / 2X	General Purpose O	FLASH LED
GPIO2	54	I/O	CMOS / 2X	General Purpose I/O	CT125/RI1
GPIO3	51	I/O	CMOS / 2X	General Purpose I/O	CT109/DCD1

3.10 Activity status indication

The activity status indication signal can be used to drive a LED through an open collector transistor according to the Wireless CPU activity status.

LED status	WISMO Quik Q24NG sub-series status	
OFF	Wireless CPU in download mode or Wireless CPU OFF	
ON	Permanent	Wireless CPU switched ON, not registered on the network
	Slow flash LED ON for 200 ms, OFF for 2 s	Wireless CPU switched ON, registered on the network
	Quick flash LED ON for 200 ms, OFF for 600 ms	Wireless CPU switched ON, registered on the network, communication in progress

Pin description

Signal	Pin number	I/O	I/O type	Description
FLASH LED	52	O	Open Drain Output	LED driving

3.11 Analog to Digital Converter (ADC)

An Analog to Digital Converter is provided by the Wireless CPU Q24NG sub-series. This converter is 10-bit resolution, ranging from 0 to 2.8 V.

Pin description

Signal	Pin number	I/O	I/O type	Description
AUXV0	33	I	Analog	A/D converter

Electrical Characteristics

Parameter	Min	Max	Unit
Resolution	10		bits
Sampling period	10		s
Input signal range	0	2.8V	V
ADC Reference Accuracy	0.75	2	%
Integral Accuracy	+/- 1		LSB
Differential Accuracy	+/- 1		LSB
Input Impedance (R)	10		MΩ
Input Impedance (C)		100	nF

3.12 Audio interface

Two different microphone inputs and two different speaker outputs are supported.

The Wireless CPU Q24NG sub-series also includes an echo cancellation feature which allows hands-free operation.

In some cases, ESD protection must be added on the audio interface lines.

3.12.1 Microphone inputs

The MIC2 inputs already include the biasing for an electret microphone allowing easy connection to a handset.

The MIC1 inputs do not include an internal bias. MIC1/SPK1 is then appropriate for a hands-free system or a handset with biasing external to the Wireless CPU.

3.12.1.1 Common microphone input characteristics

The connection can be either differential or single-ended, but using a differential connection in order to reject common mode noise and TDMA noise is strongly recommended. When using a single-ended connection, be sure to have a good ground plane, as good filtering and shielding in order to avoid any disturbance on the audio path.

Internal audio filter characteristics

Frequency	Gain
0-150 Hz	< -22 dB
150-180 Hz	< -11 dB
180-200 Hz	< -3 dB
200-3700 Hz	0 dB
>4000 Hz	< -60 dB

The gain of the MIC inputs is internally adjusted and can be tuned from 30 dB to 51 dB using an AT command (refer to the AT commands documentation [5]).

Microphone gain vs Max input voltage (using controller 1*)

Transmit Gain (dB)	Max Vin (mVrms)
+30	43.80
+33	31.01
+36	21.95
+39	15.54
+42	11
+45	7.79
+48	5.51
+51	3.9

* for more details, refer to the AT commands documentation [5]

Microphone gain vs Max input voltage (using controller 2*)

Transmit Gain (dB)	Max Vin (mVrms)	Transmit Gain (dB)	Max Vin (mVrms)
-6.5 to -4	2274	18.8 to 21.3	123.4
-3.5 to -2	1806	21.8 to 24.3	87.39
-1.5 to 0	1434	24.8 to 27.3	61.87
0.5 to 2	1139	27.8 to 30.3	43.8
2.5 to 4	905	30.8 to 33.3	31.01
4.5 to 6	719	33.8 to 36.3	21.95
6.5 to 8	571	36.8 to 39.3	15.54
8.5 to 10	454	39.8 to 42.3	11
10.8 to 12.3	348	42.8 to 45.3	7.79
12.8 to 15.3	246.3	45.8 to 48.3	5.51
15.8 to 18.3	174.4	48.8 to 51.3	3.9

* for more details, refer to the AT commands documentation [5]

3.12.1.2 Main Microphone Inputs (MIC2)

The MIC2 inputs are differential inputs. They already include convenient biasing for an electret microphone (0.5 mA and 2 Volts). This electret microphone can be directly connected to these inputs.

The impedance of microphone 2 has to be around 2 kΩ. These inputs are the standard inputs for a handset design while MIC1 inputs can be connected to an external headset or a hands-free kit.

AC coupling is already embedded in the Wireless CPU.

Pin description

Signal	Pin #	I/O	I/O type	Description
MIC2P	46	I	Analog	Microphone 2 positive input
MIC2N	48	I	Analog	Microphone 2 negative input

3.12.1.3 Auxiliary Microphone Inputs (MIC1)

The MIC1 inputs are differential and do not include internal bias. To use these inputs with an electret microphone, bias has to be generated outside the Wireless CPU Q24NG sub-series module according to the characteristic of this electret microphone. These inputs are the standard inputs used for an external headset or a hands-free kit.

The impedance of microphone 1 has to be around 2 kΩ. These inputs are provided for an external headset or a hands-free kit.

AC coupling is already embedded in the Wireless CPU.

Pin description

Signal	Pin #	I/O	I/O type	Description
MIC1P	42	I	Analog	Microphone 1 positive input
MIC1N	44	I	Analog	Microphone 1 negative input

3.12.2 Speaker outputs

3.12.2.1 Common speaker output characteristics

The connection can be differential or single-ended, but using a differential connection to reject common mode noise and TDMA noise is strongly recommended. Moreover in single-ended mode, half of the power is lost. When using a single-ended connection, be sure to have a very good ground plane, a good filtering and shielding in order to avoid any disturbance on the audio path.

Speaker outputs SPK1 and SPK2 are push-pull amplifiers and can be loaded down to 150Ω and up to 1 nF (see details in table *Speaker gain vs. Max output voltage).*

Impedance of the speaker amplifier output in differential mode is:

R ≤ 1Ω +/-10 %.

These outputs are differential and the output power can be adjusted by step of 2 dB. The output can be directly connected to a speaker.

Using a single-ended connection also includes losing half of the output power compared to a differential connection.

The gain of the speaker outputs is internally adjusted and can be tuned using an AT command.

Speaker gain vs. Max output voltage

Receive Gain (dB)*	Max output level (Vrms)	Max.speaker load (Ω)
+2	1.74	150
0	1.38	50
-2	1.099	32
-4	0.873	32
-6	0.693	32
-8	0.551	32
-10	0.437	32
-12	0.347	32
-14	0.276	32
-16	0.219	32
-18	0.174	32
-20	0.138	32
-22	0.110	32
-24	0.087	32
-26	0.069	32

* analog gain: may not be significant

3.12.2.2 Speaker 2 Outputs

Pin description

Signal	Pin #	I/O	I/O type	Description
SPK2P	45	O	Analog	Speaker 2 positive output
SPK2N	47	O	Analog	Speaker 2 negative output

3.12.2.3 Speaker 1 Outputs

Pin description

Signal	Pin #	I/O	I/O type	Description
SPK1P	41	O	Analog	Speaker 1 positive output
SPK1N	43	O	Analog	Speaker 1 negative output

3.12.3 Buzzer Output

The buzzer output is a digital output. A buzzer can be directly connected between this output and VBATT. The maximum current is 100 mA (PEAK). A diode against transient peak voltage must be connected as described below.

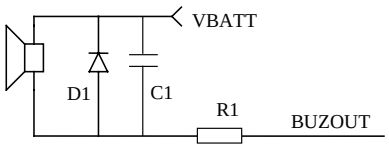


Figure 4: Buzzer connection

R1 = **TBD**

C1 = 0 to 100 nF (depending on the buzzer type).

Pin description

Signal	Pin #	I/O	I/O type	Description
BUZZER	49	O	Analog	Buzzer output

Operating conditions

Parameter	Condition	Min	Max	Unit
VOL	Iol = 100mA		0.4	V
IPEAK	VBATT = VBATTmax		100	mA

3.13 Battery charging interface

3.13.1 Hardware description

The Wireless CPU Q24NG sub-series supports one battery charging circuit for Li-Ion batteries.

This circuit uses an interface which consists of a current source inputs (CHG_IN) where the constant current has to flow in order to charge the battery.

This current value depends on battery capacity. It is recommended to provide a current equal to the value of the capacity plus 50 mA. For a 550 mA battery the current will be 600 mA. The maximum current is 800 mA.

A specific AT command (**AT+WBCM**), available from 4.3 level, allows the battery charge to be managed (start and stop the charge, enable or disable unsolicited Battery Charge Indications and set the battery charge parameters).

The Wireless CPU Q24NG sub-series monitors the battery voltage to detect the end of the charge.

The Wireless CPU Q24NG sub-series also monitors the temperature of the battery through the BAT_TEMP pin which must be connected to a temperature sensor inside the battery (a NTC resistor for instance).

Pin description

Signal	Pin number	I/O	I/O type	Description
CHG_IN	1, 2, 4	I	Supply	Current source input
BAT_TEMP	38	I	Analog	A/D converter

Electrical Characteristics

Parameter	Min	Max	Typ	Unit
BAT_TEMP resolution	10			bits
BAT_TEMP sampling rate	90.3			Ksps/s
BAT_TEMP Input Impedance (R)	4.7			kΩ
BAT_TEMP Input Impedance (C)		100		nF
CHG_IN Voltage (for I=Imax)	4.6*	6		V
CHG_IN Current		800		mA
BAT_TEMP Input signal range			2.8	Vpp

To be configured as per battery manufacturer

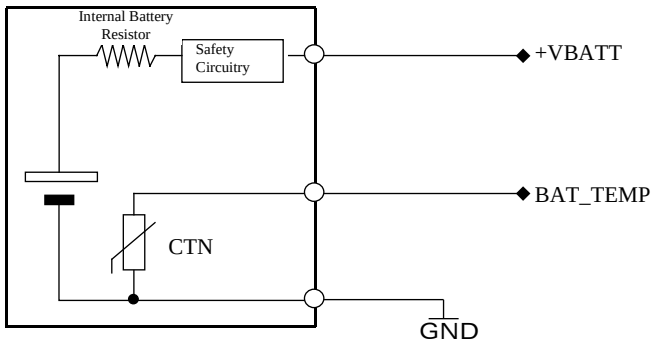


Figure 5: Connection examples

3.13.2 Li-ion charging procedure

A constant current source has to be provided through CHG_IN inputs in order to charge the Li-ion battery, and BAT_TEMP input has to be connected to a battery temperature sensor. During this procedure the voltage of the battery is accurately monitored.

Li-ion charging involves two phases:

- During the first phase, the battery is charged with a constant current until its voltage reaches **4.1 V***,
- During the second phase, the constant current is pulsed by the Wireless CPU. The width and the frequency of the pulse change during this phase in order to ensure a safety charge.

The battery is considered as fully charged.

- after a pulse,
- and if the voltage remains at a **4.1 V*** for more than 10 s.

The Li-ion battery must have a safety circuit included to avoid any discharge or overcharge. This circuit is delivered by the manufacturer inside the battery pack. The impedance of this safety circuit has to be the lowest possible in order to reduce the voltage drop-out. This drop-out is due to the RF Power Amplifier current (up to 2.0 A). A maximum of 150 mΩ is required.

* To be configured as per the battery manufacturer.

3.14 ON / ~OFF

3.14.1 General description

This input is used to switch ON or OFF the Wireless CPU Q24NG.

A high level signal has to be provided on the ON/~OFF pin to switch ON the Wireless CPU.

The voltage level of this signal has to be maintained between 2.4 V and VDD for a minimum of 1 s.

This signal can be left at high level until switched OFF.

To be able to switch OFF the Wireless CPU, the pin ON/~OFF has to be released. Through the firmware, the Wireless CPU can be switched OFF (using the AT+CPOF command).

Pin description

Signal	Pin number	I/O	I/O type	Description
ON/~OFF	6	I	CMOS	Wireless CPU Power ON/OFF

Electrical Characteristics

Parameter	Min	Max	Unit
Input Impedance (R)	10		kΩ
Input Impedance (C)		50	pF

Operating conditions

Parameter	I/O type	Min	Max	Unit
VIL	CMOS		VBATT x 0.2	V
VIH	CMOS	VBATT x 0.8	VBATT + 0.3V	V

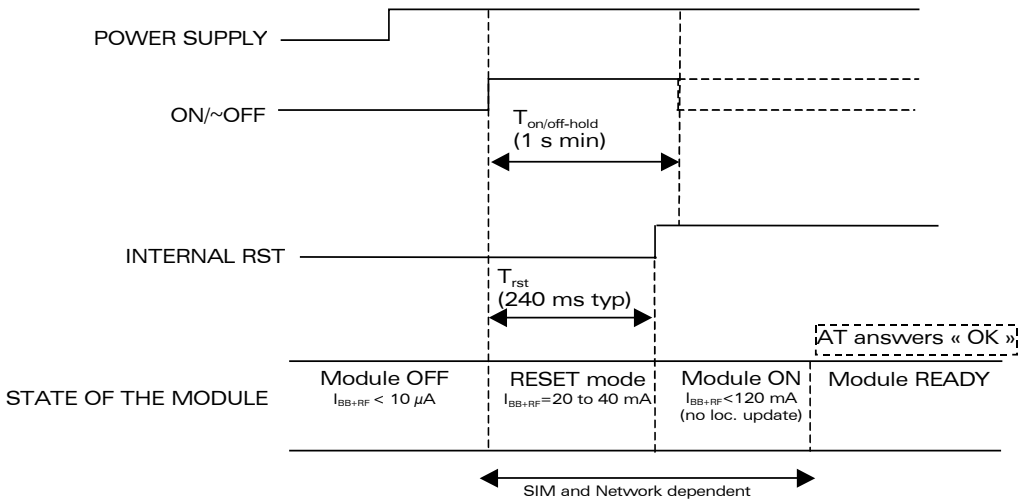
3.14.2 Operating sequences

3.14.2.1 Power ON

Once the Wireless CPU is supplied by the power source, the application must set the ON/~OFF signal to high to start the Wireless CPU power ON sequence.

The ON/~OFF signal must be held for 1 sec minimum. After this time, an internal mechanism maintains this on hold condition. During the power ON sequence, an internal reset is automatically performed by the Wireless CPU for 240 ms (typical). During this phase, any external reset should be avoided.

Once initialization is complete (timing is SIM and network dependent) the AT interface answers "OK" to the application[1]. For further details, please refer to the AT commands documentation (AT+WIND, AT+WAIP)



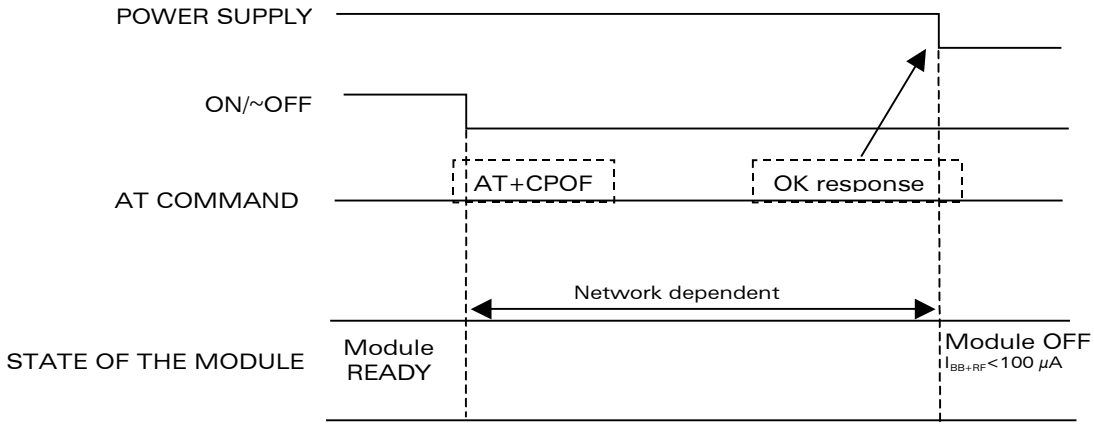
I_{BB+RF} = overall current consumption (Base Band + RF part)

Figure 6: Power-ON sequence diagram (no PIN code activated)

[1] For this, the application has to send AT↵. If the application manages hardware flow control, the AT command can be sent during the initialisation phase. Another solution is to use the AT+WIND command to get an unsolicited status from the Wireless CPU.

3.14.2.2 Power OFF

To power OFF the Wireless CPU correctly, the application must set the ON/~OFF signal to low and then send the AT+CPOF command to de-register from the network and switch off the Wireless CPU. Once the "**OK**" response is issued by the Wireless CPU, the power supply can be switched off.



I_{BB+RF} = overall current consumption (Base Band + RF part)

Figure 7: Power-OFF sequence diagram

3.15 BOOT (optional)

This input can be used to download software to the Flash memory of the Wireless CPU Q24NG sub-series.

For applications based on AT commands, this is a backup download procedure (refer to document [3] Customer Design Guidelines).

The internal boot procedure is started when this pin is low during Wireless CPU reset.

In normal mode this pin must be left open. In Internal boot mode, low level has to be set through a 1KΩ resistor. If used, this input has to be driven by an open collector or an open drain output:

- BOOT pin 12 = 0, for download mode,
- BOOT pin 12 = 1, for normal mode.

Pin description

Signal	Pin number	I/O	I/O type	Description
BOOT	12	I	CMOS	Flash Downloading

Note:

The nominal firmware download procedure is using the X-modem.

3.16 Reset signal (~RST)

3.16.1 General description

This signal is used to force a reset procedure by providing low level for at least 500 µs.

This signal must be considered as an emergency reset only. A reset procedure is automatically driven by the internal hardware during the power-up sequence.

This signal can also be used to provide a reset to an external device. It then behaves as an output. If no external reset is necessary this input can be left open. If used (emergency reset), it mustbe driven by an open collector or an open drain output:

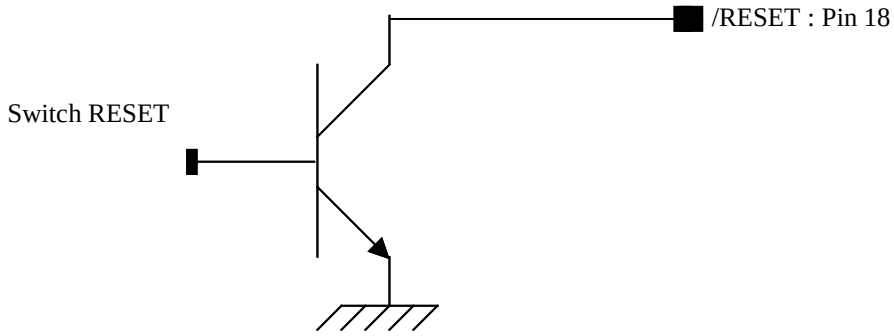


Figure 8: RST pin connection

- ~RST pin 14 = 0, for Wireless CPU Reset,
- ~RST pin 14 = 1, for normal mode.

Pin description

Signal	Pin number	I/O	I/O type	Description
~RST	14	I/O	SCHMITT	Wireless CPU Reset

Electrical Characteristics

Parameter	Min	Max	Unit
Input Impedance (R)	4.7		kΩ
Input Impedance (C)		10	nF

Operating conditions

Parameter	Min	Max	Condition
*VT-	1.1 V	1.2 V	
*VT+	1.7 V	1.9 V	
VOL		0.4 V	IOL = -50 µA
VOH	2.0 V		IOH = 50 µA

* V_{T-}, V_{T+} : Hysteresis thresholds

Additional comments on RESET:

The RESET process is activated either by the external ~RST signal or by an internal signal (coming from a RESET generator). This automatic reset is activated during a power-up sequence.

The Wireless CPU remains in RESET mode as long as the ~RST signal is held low.

This signal should be used only for "**emergency**" resets.

A software reset is always preferred to a hardware reset.

3.16.2 Reset sequence

To activate the "**emergency** "reset sequence, the ~RST signal has to be set to low for 500 µs minimum.

As soon as the reset is complete, the AT interface answers "**OK** " to the application. In this case, the application has to send AT↵. If the application manages hardware flow control, the AT command can be sent during the initialization phase. Another solution is to use the AT+WIND command to obtain an unsolicited status from the Wireless CPU.

For further details, refer to the AT commands documentation [5].

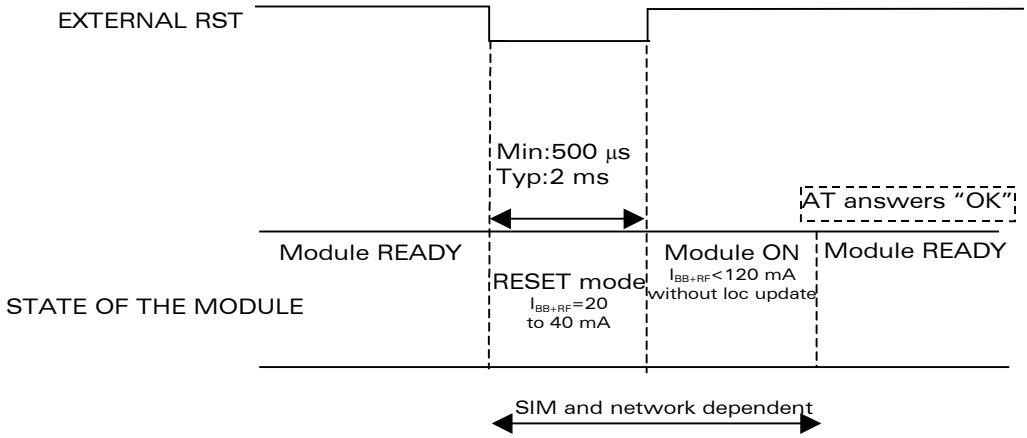


Figure 9: Reset sequence diagram

3.17 External Interrupt (~INTR)

The Wireless CPU Q24NG sub-series provides an external interrupt input ~INTR. This input is highly sensitive and an interrupt is activated on the high to low edge. If this signal is not used it can be left open. If used this input has to be driven by an open collector or an open drain output.

This input is used for example, to automatically power OFF the Wireless CPU.

Pin description

Signal	Pin number	I/O	I/O type	Description
~INTR	16	I	CMOS	External Interrupt

Electrical characteristics

Parameter	Min	Max	Unit
VIL	-0.5	0.7	Volt
VIH	2.2	3.0	Volt

3.18 VCC output

This output can be used to power some external functions. VCC must be used as a digital power supply. This power supply is available when the Wireless CPU is ON.

Pin description

Signal	Pin number	I/O	I/O type	Description
VCC	40	O	Supply	Digital supply

Operating conditions

Parameter	Condition	Min	Max	Unit
Output voltage	I = 100 mA	2.74	2.86	V
Output Current			100	mA

3.19 Real Time Clock Supply (VCC_RTC)

The VCC_RTC input is used to provide a back-up power supply for the internal Real Time Clock. The RTC is supported by the Wireless CPU when powered on but a back-up power supply is needed to save date and time information when the Wireless CPU is switched off.

If the RTC is not used, this pin can be left open.

Pin description

Signal	Pin number	I/O	I/O type	Description
VCC_RTC	56	I/O	Supply	RTC Back-up supply

Operating conditions

Parameter	Condition	Min	Max	Unit
Input voltage		2	2.75	V
Input Current	VCC=0 V; t° = +25°C VCC_RTC=2.5 V		3	µA
Input Current	VCC=0 V; t°:-20°C / +55°C VCC_RTC=2.5 V		10	µA
Output voltage		2.4	2.75	V
Output current			2	mA

3.20 RF interface

The impedance is 50Ω nominal and the DC impedance is 0Ω.

3.20.1 RF connections

The RF connection can be made by different connections.

- U.FL Connector (on both sides)

  A wide variety of cables fitted with U.FL connectors is proposed by different suppliers.

- MMS Connector

  The MMS connector stands on three pliable legs. The design guarantees the receptacle stability after placement. The MMS snap on mating system ensures a correct positive connection each time.

  A wide variety of cables fitted with MMS connectors is proposed by different suppliers.

- Soldered solution

  The soldered solution will preferably be based on an RG178 coaxial cable.

- IMP connector

  This connector is dedicated to different board applications and must be soldered to the customer board. The supplier is Radiall with the following reference : **R107 064 900** or **R107 064 920**.

Notes:

- The Wireless CPU Q24NG does not support an antenna switch for a car kit but this function can be implemented externally and it can be driven using a GPIO.
- The antenna cable and connector should be chosen in order to minimize losses in the frequency bands used for GSM 850/900MHz and 1800/1900MHz.
- 0.5dB can be considered as a maximum value for loss between the Wireless CPU and an external connector.
- In order to maintain the RoHS status of the Wireless CPU, Wavecom recommend for the assembly of the Wireless CPU on the mother board and the assembly of RF cable on to use the lead free solder wire and flux.

  Example:

  o Solder Wire: Kester 245 Cored 58 (Sn96.5Ag3Cu0.5)

  o Flux: Kester 952-D6

3.20.2 RF performances

RF performance is compliant with the ETSI recommendation ETSI TS 151 010-1.

The main parameters for Receivers are:

- SM850 Reference Sensitivity = -104 dBm Static & TUHigh
- EGSM900 Reference Sensitivity = -104 dBm Static & TUHigh
- DCS1800 Reference Sensitivity = -102 dBm Static & TUHigh
- PCS1900 Reference Sensitivity = -102 dBm Static & TUHigh
- Selectivity @ 200 kHz : > +9 dBc
- Selectivity @ 400 kHz : > +41 dBc
- Linear dynamic range : 63 dB
- Co-channel rejection : >= 9 dBc

And for Transmitters:

- Maximum output power (EGSM & GSM850): 33 dBm +/- 2 dB at ambient temperature
- Maximum output power (GSM1800 & PCS1900) : 30 dBm +/- 2 dB at ambient temperature
- Minimum output power (EGSM & GSM850) : 5 dBm +/- 5 dB at ambient temperature
- Minimum output power (GSM1800 & PCS1900) : 0 dBm +/- 5 dB at ambient temperature

3.20.3 Antenna specifications

The antenna must fulfill the following requirements:

- The optimum operating frequency depends on the application. A dual band or a quad band antenna must operate in these frequency bands and have the following characteristics:

Characteristic		Q24NG			
		EGSM 900	DCS 1800	GSM 850	PCS 1900
TX Frequency		880 to 915 MHz	1710 to 1785 MHz	824 to 849 MHz	1850 to 1910 MHz
RX Frequency		925 to 960 MHz	1805 to 1880 MHz	869 to 894 MHz	1930 to 1990 MHz
Impedance		50Ω			
VSWR	Rx max	1.5 :1			
	Tx max	1.5 :1			
Typical radiated gain		0dBi in one direction at least			

4 Technical specifications

4.1 General Purpose Connector pin-out description

Pin #	Name	I/O	I/O type	Description	Comment
1	CHG_IN	I	Supply	Supply for battery charging	High current
2	CHG_IN	I	Supply	Supply for battery charging	High current
3	SIM_CLK	O	2 X	Clock for SIM interface	
4	CHG_IN	I	Supply	Supply for battery charging	High current
5	SIM_RST	O	2 X	Reset for SIM interface	
6	ON/~OFF	I	CMOS	Power ON/OFF control	
7	SIM_DATA	I/O	CMOS / 3X	I/O for SIM interface	
8	SDA/SPI_IO	I/O	CMOS/1X	Wire interface or SPI Serial Data	
9	SIM_VCC	O	Supply	SIM card supply	6 mA max
10	SCL/SPI_CLK	O	1X	Wire interface or SPI Serial clock	
11	VDD	I	Supply	Low power supply	3.1 V minimum or connected to VBATT
12	BOOT	I	CMOS	BOOT	Pull down through 1 KΩ for Flash downloading
13	ROW0	I/O	CMOS/1X	Keyboard Row	
14	~RST	I/O	SCHMITT	Wireless CPU Reset	Active low
15	ROW1	I/O	CMOS/1X	Keyboard Row	
16	~INTR	I	CMOS	External interrupt	Active low. 100 KΩ Pull-up inside
17	ROW2	I/O	CMOS/1X	Keyboard Row	
18	GPI or CT103/TXD2	I	CMOS or 3x	General Purpose Input or Aux.serial Link (UART2)	100K Pull-down inside - Multiplexed
19	ROW3	I/O	CMOS/1X	Keyboard Row	
20	GPO2 or CT104/RXD2	O	1X or CMOS	General Purpose Output or Aux.serial Link (UART2)	Multiplexed
21	ROW4	I/O	CMOS/1X	Keyboard Row	
22	GPO1	O	3X	General Purpose Output	
23	COL0	I/O	CMOS/1X	Keyboard Column	
24	GPIO0 or CT106/CTS2	I/O	CMOS/2X or CMOS	General Purpose I/O or Aux. serial Link (UART2)	Multiplexed
25	COL1	I/O	CMOS/1X	Keyboard Column	

Pin #	Name	I/O	I/O type	Description	Comment
26	GPO0 or SPI_AUX	O	3X or 1X	General Purpose Output or SPI Aux Or SIM 3 V / 5 V	Multiplexed
27	COL2	I/O	CMOS/1X	Keyboard Column	
28	SPI_EN or GPO3	O	1X or CMOS	SPI enable or General Purpose Output	Multiplexed
29	COL3	I/O	CMOS/1X	Keyboard Column	
30	CT105/RTS1	I	CMOS	Serial link interface Request To Send (UART1)	Pull up to VCC with 100 kΩ when not used
31	COL4	I/O	CMOS/1X	Keyboard Column	
32	CT104/RXD1	O	1X	Serial link interface Receive (UART1)	
33	AUXV0	I	Analog	Auxiliary ADC input 0	Can be tied to GND if not used
34	CT108-2/DTR1	I	CMOS	Serial link interface Data Terminal Ready (UART1)	Pull up to VCC with 100 kΩ when not used
35	GPIO5 or CT105/RTS2	I/O	CMOS / 2X or 2X	General Purpose I/O or Aux. serial Link (UART2)	Multiplexed
36	CT107/DSR1	O	1X	Serial link interface Data Set Ready (UART1)	
37	CT106/CTS1	O	1X	Serial link interface Clear To Send (UART1)	
38	BAT_TEMP	I	Analog	ADC input for battery temperature measurement	Can be tied to GND if not used
39	CT103/TXD1	I	CMOS	Serial link interface Transmit (UART1)	Pull up to VCC with 100 kΩ when not used
40	VCC	O	Supply	2.8 V digital supply output	100 mA max.
41	SPK1P	O	Analog	Speaker 1 positive output	
42	MIC1P	I	Analog	Microphone 1 positive input	
43	SPK1N	O	Analog	Speaker 1 negative output	
44	MIC1N	I	Analog	Microphone 1 negative input	
45	SPK2P	O	Analog	Speaker 2 positive output	
46	MIC2P	I	Analog	Microphone 2 positive input	
47	SPK2N	O	Analog	Speaker 2 negative output	

Pin #	Name	I/O	I/O type	Description	Comment
48	MIC2N	I	Analog	Microphone 2 negative input	
49	BUZZER	O	Analog	Buzzer output	100 mA max
50	SIM_PRES	I	CMOS	SIM Card Detect	
51	GPIO3 or CT109/DCD1	I/O O	CMOS/2X	General Purpose I/O Serial interface Data Carrier Detect (UART1)	Multiplexed
52	GPIO1 FLASH LED	I/O	CMOS/2X	General Purpose I/O Wireless CPU State	Multiplexed
53	GPIO4	I/O	CMOS/2X	General Purpose I/O	
54	GPIO2 or CT125 / RI1	I/O O	CMOS/2X	General Purpose I/O Serial interface Ring Indicator (UART1)	Multiplexed
55	+VBATT		Supply	Battery Input	High current
56	VCC_RTC	I/O	Supply	RTC back-up supply	
57	+VBATT		Supply	Battery Input	High current
58	+VBATT		Supply	Battery Input	High current
59	+VBATT		Supply	Battery Input	High current
60	+VBATT		Supply	Battery Input	High current

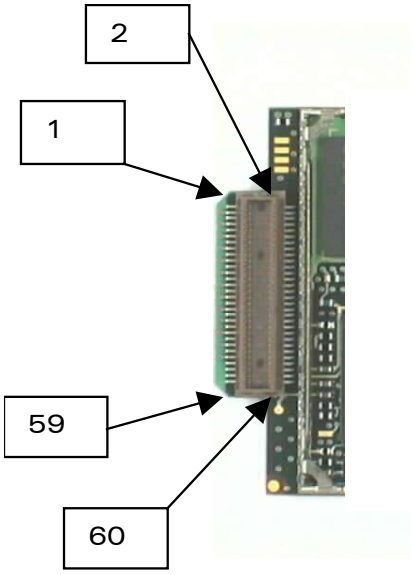


Figure 10: Wireless pin position (bottom view)

Environmental Specifications

In Wireless CPU Q24NG, Q24 Classic and Q24 Plus are compliant with the following operating classes:

Conditions	Temperature range
Operating / Class A	-20°C to +55°C for GSM 850 / 900 -10°C to +55°C for GSM 1800/1900
Storage	-40°C to +85°C

In Wireless CPU Q24NG, Q24 Automotive and Q24 Extended are compliant with the following operating classes:

Conditions	Temperature range
Operating / Class A	-20°C to +55°Cfor GSM 850 / 900 -10°C to +55°C for GSM 1800/1900
Operating / Class B	-30°C to +75°C
Operating / Class C	-40°C to + 85°C
Storage	-40° to + 85°C

Function Status Classification:

- Class A:

The Wireless CPU shall have full function during and after an external influence. The GSM performance shall meet the minimum ETSI requirements.

- Class B:

Any functions can be out of specified tolerances. All the functions will be going back to normal tolerances automatically after the external influence has been removed. Performance is allowed to go outside of the minimum ETSI requirements but it must be possible to connect a call and send an SMS.

- Class C:

The functional requirements will not be fulfilled during external influence, but will return to full function automatically after the external influence has been removed.

4.1.1 Environmental qualification

For Wireless CPU Q24NG, Q24 Classic, Q24 Plus and Q24 Extended, environmental qualifications applied are defined in the table below:

		ENVIRONMENTAL CLASSES		
TYPE OF TEST	STANDARDS	STORAGE Class 1.2	TRANSPORTATION Class 2.3	OPERATING (PORT USE) Class 7.3
Cold	IEC 68-2.1 Ab test	-25° C 72 h	-40° C 72 h	-20° C (GSM900) 16 h -10° C (GSM1800/1900) 16h
Dry heat	IEC 68-2.2 Bb test	+70° C 72 h	+70° C 72 h	+55° C 16 h
Change of temperature	IEC 68-2.14 Na/Nb test		-40° / +30° C 5 cycles t1 = 3 h	-20° / +30° C (GSM900) 3 cycles -10° / +30° C (GSM1800/1900): 3 cycles t1 = 3 h
Damp heat cyclic	IEC 68-2.30 Db test	+30° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1	+40° C 2 cycles 90% - 100% RH variant 1
Damp heat	IEC 68-2.56 Cb test	+30° C 4 days	+40° C 4 days	+40° C 4 days
Sinusoidal vibration	IEC 68-2.6 Fc test	5 - 62 Hz : 5 mm / s 62 - 200Hz : 2 m / s2 3 x 5 sweep cycles		
Random vibration wide band	IEC 68-3.36 Fdb test		5 - 20 Hz : 0.96 m2 / s3 20 - 500Hz : - 3 dB / oct 3 x 10 min	10 -12 Hz : 0.96 m2 / s3 12 - 150Hz : - 3 dB / oct 3 x 30 min

Figure 11: Q24 Classic, Q24 Plus and Q24 extended Environmental classes

For more details refer to the document: Environmental Control Plan For Wireless CPU Q24NG [2]

Electro-Static Discharge (ESD):

According to the norm **EN 61000-4-2**, the maximum ESD level supported by the Q24x6 sub-series on contact discharges is ±1 kV on the 60 pin connector and ±2 kV on the antenna connector.

Humidity:

According to **IPC/JEDEC J-STD-033**, the moisture class of the Q2400 series is **level 3**. The floor life from the time of opening of the sealed bag is 168 hours.

For Wireless CPU Q24NG: Q24 Automotive, environmental qualification applied is defined in under table:

Test Designation	Standards	Definition / Severities
Resistance to Heat	IEC 60068-2-2	Temperature: +85°C Duration: 504 h
Resistance to cold test	IEC 60068-2-30 Db	Storage temperature: -40±2°C Storage time: 72 h
Cooking Test	-	Temperature: +70 ±2°C Duration: 100 days
Damp heat test	IEC 60068-2-3	Storage temperature: +40±2°C Storage humidity: 95±3% Storage time: 21 days
Damp heat cycle test	IEC 60068-2-30 Db	Upper temperature: +55±2°C Number of cycles: 10
Temperature change	IEC 60068-2-14 Nb	Low temperature: -40°±2°C High temperature: +85±2°C Total duration: 11 days
Thermal Shock	IEC 60068-2-14	Low temperature: -40°±2°C High temperature: +85±2°C Total duration: 200 hours
Resistance to sinusoidal vibration	IEC 60068-2-6 Fc	[10 Hz to 16 Hz]: ±5 mm (peak) [16 Hz to 62 Hz]: 5 g (peak) [62 Hz to 200Hz]: 3g (peak) [200 Hz to 1000 Hz] 1g (peak) Test duration: 20 cycles Sweep directions: X / Y / Z
Resistance to random vibration	IEC 60068-2-64	Frequency range: 10 Hz - 2000 Hz Spectrum level: 0.1 g^2/Hz at 10 Hz 0.01 g^2/Hz at 250 Hz 0.0005 g^2/Hz at 1000 Hz 0.0005 g^2/Hz at 2000 Hz Duration: 16 h Vibration axis: X / Y / Z
Resistance to mechanical shock	IEC 68-2-27	Peak acceleration: 30g / 100g / 200g Direction: ±X, ±Y, ±Z
ESD Test	IEC 1000-4-2	1 kV contact discharge on 60-pin connector 2 kV contact discharge on RF connector

Figure 12: Q24 automotive Environmental classes

For more details refer to the document:

"Automotive Environmental Control" Plan For Wireless CPU Q24NG [1]

4.1.2 Reflow soldering:

The Wireless CPU Q24NG series does not support any reflow soldering.

4.2 Mechanical specifications

4.2.1 Physical characteristics

The Wireless CPU Q24NG sub-series has a complete self-contained shield.

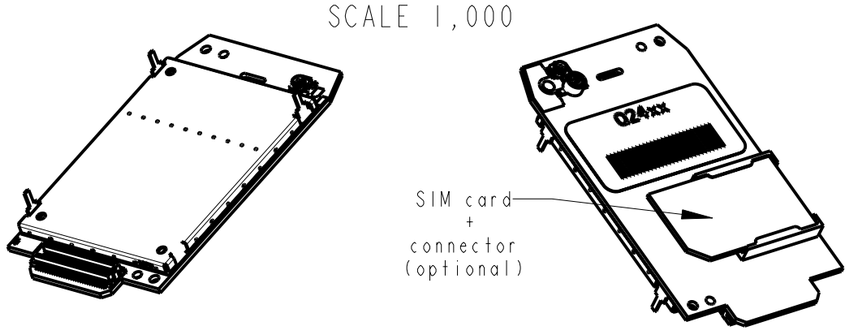
• Dimensions	:	58.4 x 32.2 x 3.9 mm external dimensions (excludingshielding pins)
• Weight	:	<11 g (12g for Q24 Automotive)

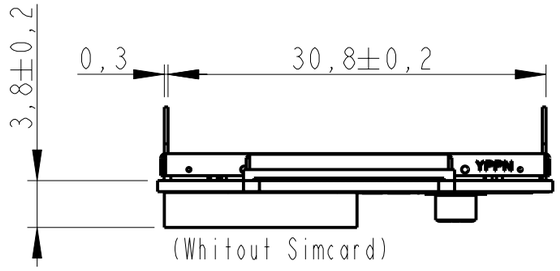
4.2.2 Mechanical drawings

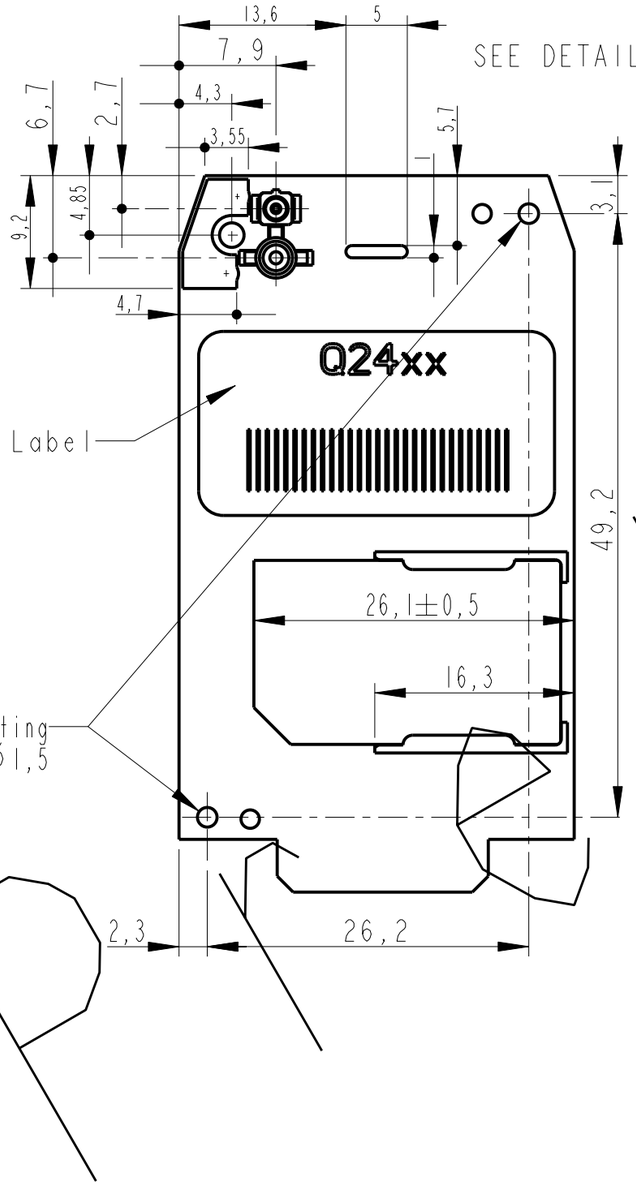
The next page gives the mechanical specifications of the Wireless CPU Q24NG sub-series.

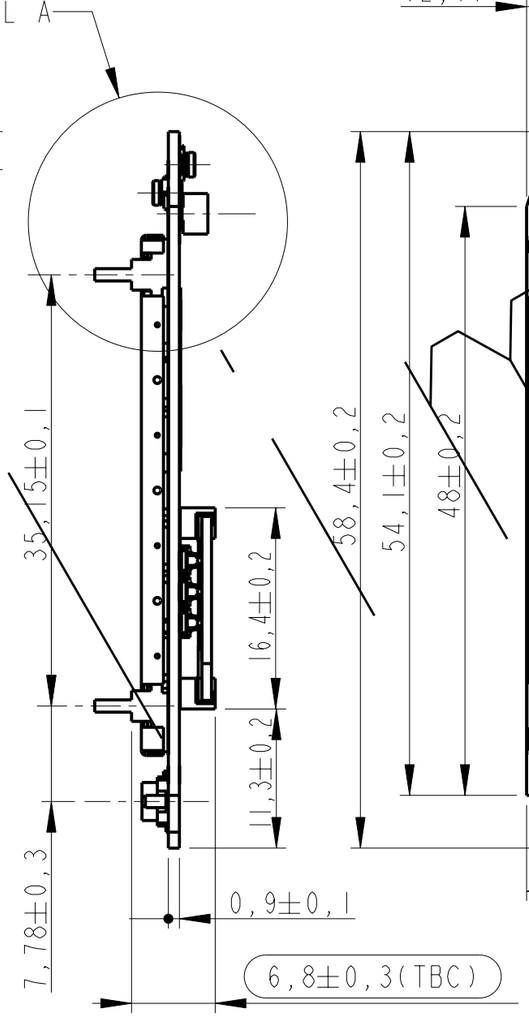
Figure 13: Mechanical drawing

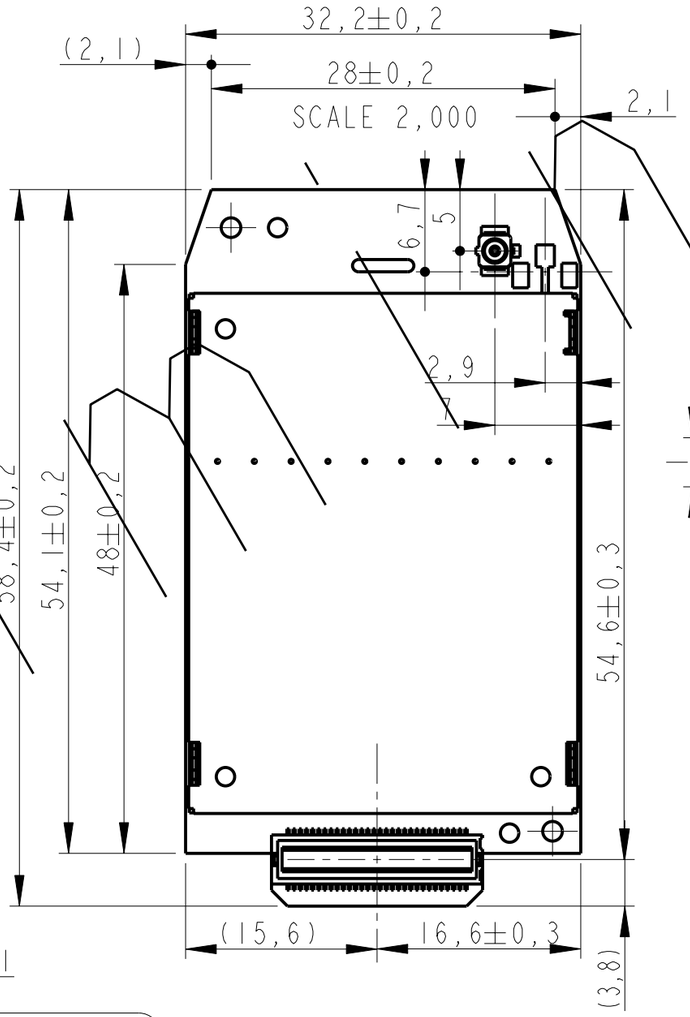
SCALE 1,000

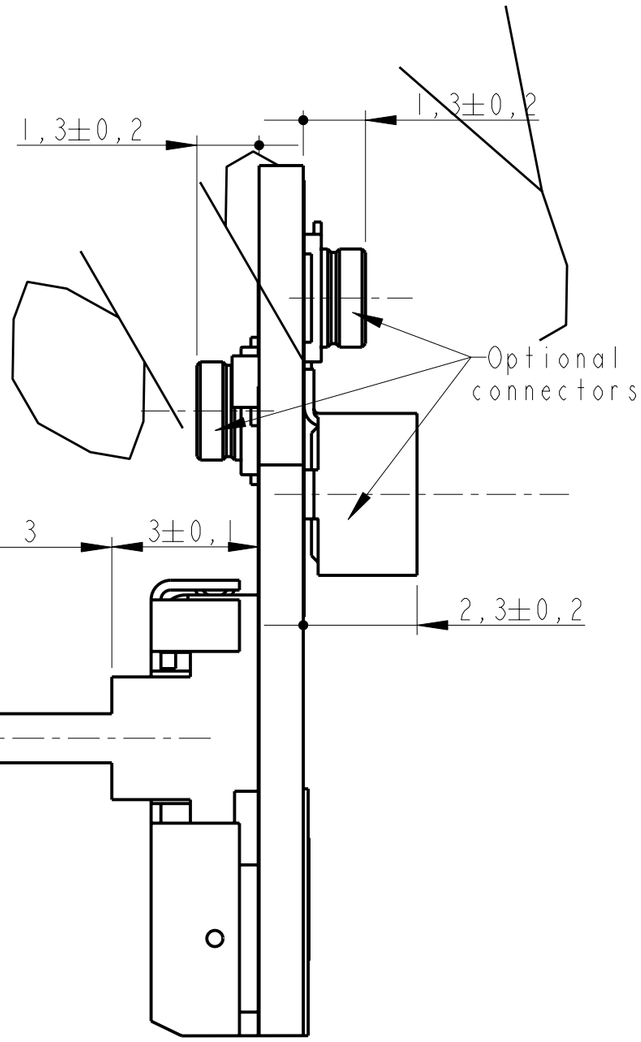












DETAIL A
SCALE 8,000

MODIFICATION	DATE	AUTHOR	RESP.	STATUS	IND
Update:GND/oblong	07/04/06	JPM	ASC	Prototypes	02
Creation	30/03/06	JPM	ASC	Prototypes	01

Q24 NG	GEN.TOL. : ±0,1		SCALE : 1,000	
MODULE DIMENSIONS	DOC.	FOLIO: 1/1	FORMAT : A3	
	WM-3-600101-V-003-A			
wavecom	AUTHOR : JPM			
	RESPONS : ASC			02
PRO/ENGINEER MODULE				IND.

5 Connector and peripheral device references

5.1 General Purpose Connector data sheet

The supplier for the GPC connector is KYOCERA/ELCO, available from http://www.avxcorp.com .

5.2 SIM Card Reader

- ITT CANNON CCM03 series (see http://www.ittcannon.com)
- AMPHENOL C707 series (see http://www.amphenol.com)
- JAE (see http://www.jae.com)

Drawer type:

- MOLEX 99228-0002 (connector) / MOLEX 91236-0002 (holder) (see http://www.molex.com)

5.3 Microphone

Potential suppliers:

- HOSIDEN
- PANASONIC
- PEIKER

5.4 Speaker

Potential suppliers:

- SANYO
- HOSIDEN
- PRIMO
- PHILIPS

5.5 Antenna Cable

The following cable reference has been certified for mounting on the Wireless CPU Q24NG:

- RG178

5.6 RF board to board connector

The supplier for the IMP connector is Radiall (http://www.radiall.com) with the following reference :

- R107 064 900.
- R107 064 920.

The supplier for the MMS connector is Radiall (http://www.radiall.com)

5.7 GSM antenna

GSM antennas and support for antenna adaptation can be obtained from the manufacturers such as:

- ALLGON (http://www.allgon.com)
- HIRSCHMANN (http://www.hirschmann.com/)

6 Appendix

6.1 Standards and Recommendations

GSM ETSI, 3GPP, GCF and NAPRD03 recommendations for Phase II.

Specification Reference	Title
3GPP TS 45.005 v5.5.0 (2002-08) Release 5	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception
GSM 02.07 V8.0.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); Mobile Stations (MS) features (GSM 02.07 version 8.0.0 Release 1999)
GSM 02.60 V8.1.0 (1999-07)	Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description, Stage 1 (GSM 02.60 version 8.1.0 Release 1999)
GSM 03.60 V7.9.0 (2002-09)	Technical Specification Group Services and System Aspects; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Service description; Stage 2 (Release 1998)
3GPP TS 43.064 V5.0.0 (2002-04)	Technical Specification Group GERAN; Digital cellular telecommunications system (Phase 2+); General Packet Radio Service (GPRS); Overall description of the GPRS radio interface; Stage 2 (Release 5)
3GPP TS 03.22 V8.7.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Functions related to Mobile Station (MS) in idle mode and group receive mode; (Release 1999)
3GPP TS 03.40 V7.5.0 (2001-12)	Technical Specification Group Terminals; Technical realization of the Short Message Service (SMS) (Release 1998)
3GPP TS 03.41 V7.4.0 (2000-09)	Technical Specification Group Terminals; Technical realization of Cell Broadcast Service (CBS) (Release 1998)
ETSI EN 300 903 V8.1.1 (2000-11)	Digital cellular telecommunications system (Phase 2+); Transmission planning aspects of the speech service in the GSM Public Land Mobile Network (PLMN) system (GSM 03.50 version 8.1.1 Release 1999)
3GPP TS 04.06 V8.2.1 (2002-05)	Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station - Base Station System (MS - BSS) interface; Data Link (DL) layer specification (Release 1999)
3GPP TS 04.08 V7.18.0 (2002-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Mobile radio interface layer 3 specification (Release 1998)
3GPP TS 04.10 V7.1.0 (2001-12)	Technical Specification Group Core Networks; Mobile radio interface layer 3 Supplementary services specification; General aspects (Release 1998)
3GPP TS 04.11 V7.1.0 (2000-09)	Technical Specification Group Core Network; Digital cellular telecommunications system (Phase 2+); Point-to-Point (PP) Short Message Service (SMS) support on mobile radio interface

Specification Reference	Title
	(Release 1998)
3GPP TS 45.005 v5.5.0 (2002-08)	Technical Specification Group GSM/EDGE. Radio Access Network; Radio transmission and reception (Release 5)
3GPP TS 45.008 V5.8.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem link control (Release 5)
3GPP TS 45.010 V5.1.0 (2002-08)	Technical Specification Group GSM/EDGE Radio Access Network; Radio subsystem synchronization (Release 5)
3GPP TS 46.010 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Transcoding (Release 5)
3GPP TS 46.011 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Substitution and muting of lost frames for full rate speech channels (Release 5)
3GPP TS 46.012 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Comfort noise aspect for full rate speech traffic channels (Release 5)
3GPP TS 46.031 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Discontinuous Transmission (DTX) for full rate speech traffic channels (Release 5)
3GPP TS 46.032 V5.0.0 (2002-06)	Technical Specification Group Services and System Aspects; Full rate speech; Voice Activity Detector (VAD) for full rate speech traffic channels (Release 5)
TS 100 913V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General on Terminal Adaptation Functions (TAF) for Mobile Stations (MS) (GSM 07.01 version 8.0.0 Release 1999)
GSM 09.07 V8.0.0 (1999-08)	Digital cellular telecommunications system (Phase 2+); General requirements on inter-working between the Public Land Mobile Network (PLMN) and the Integrated Services Digital Network (ISDN) or Public Switched Telephone Network (PSTN) (GSM 09.07 version 8.0.0 Release 1999)
3GPP TS 51.010-1 v5.0.0 (2002-09)	Technical Specification Group GSM/EDGE ; Radio Access Network ;Digital cellular telecommunications system (Phase 2+);Mobile Station (MS) conformance specification; Part 1: Conformance specification (Release 5)
3GPP TS 51.011 V5.0.0 (2001-12)	Technical Specification Group Terminals; Specification of the Subscriber Identity Module - Mobile Equipment (SIM - ME) interface (Release 5)
ETS 300 641 (1998-03)	Digital cellular telecommunications system (Phase 2); Specification of the 3 Volt Subscriber Identity Module - Mobile Equipment (SIM-ME) interface (GSM 11.12 version 4.3.1)
GCF-CC V3.7.1 (2002-08)	Global Certification Forum – Certification criteria
NAPRD03 V2.6.0 (2002-06)	North America Permanent Reference Document for PTCRB tests

6.2 Safety recommendations (for information only)

Warning:

For the efficient and safe operation of your GSM applications based on the Wireless CPU Q24NG.

Please read this information carefully.

6.2.1 RF safety

6.2.1.1 General

Your GSM terminal[2] is based on the GSM standard for cellular technology. The GSM standard is spread all over the world. It covers Europe, Asia and some parts of America and Africa. This is the most used telecommunication standard.

Your GSM terminal is actually a low power radio transmitter and receiver. It sends out and receives radio frequency energy. When you use your GSM application, the cellular system which handles your calls controls both the radio frequency and the power level of your cellular modem.

6.2.1.2 Exposure to RF energy

There has been some public concern about possible health effects of using GSM terminals. Although research on health effects from RF energy has focused on the current RF technology for many years, scientists have begun research regarding newer radio technologies, such as GSM. After existing research had been reviewed, and after compliance to all applicable safety standards had been tested, it has been concluded that the product was safe to use.

If you are concerned about exposure to RF energy there are things you can do to minimize the exposure. Obviously, limiting the duration of your calls will reduce your exposure to RF energy. In addition, you can reduce RF exposure by operating your cellular terminal efficiently by following the guidelines given in the sections below.

6.2.1.3 Efficient terminal operation

For your GSM terminal to operate at the lowest power level, consistent with satisfactory call quality:

- If your terminal has an extendable antenna, extend it fully. Some models allow you to place a call with the antenna retracted. However your GSM terminal operates more efficiently with the antenna fully extended.
- Do not hold the antenna when the terminal is « IN USE ». Holding the antenna affects call quality and may cause the modem to operate at a higher power level than needed.

[2] based on WISMO2D

6.2.1.4 Antenna care and replacement

- Do not use the GSM terminal with a damaged antenna. If a damaged antenna comes into contact with the skin, a minor burn may result. Replace a damaged antenna immediately. Consult your manual to see if you may change the antenna yourself. If so, use only a manufacturer-approved antenna. Otherwise, have your antenna repaired by a qualified technician.
- Use only the supplied or approved antenna. Unauthorized antennas, modifications or attachments could damage the terminal and may contravene local RF emission regulations or invalidate type approval.

6.2.2 General safety

6.2.2.1 Driving

Check the laws and the regulations regarding the use of cellular devices in the area where you have to drive as you always have to comply with them. When using your GSM terminal while driving, please :

- give full attention to driving,
- pull off the road and park before making or answering a call if driving conditions so require.

6.2.2.2 Electronic devices

Most electronic equipment, for example in hospitals and motor vehicles is shielded from RF energy. However RF energy may affect some improperly shielded electronic equipment.

6.2.2.3 Vehicle electronic equipment

Check your vehicle manufacturer representative to determine if any on-board electronic equipment is adequately shielded from RF energy.

6.2.2.4 Medical electronic equipment

Consult the manufacturer of any personal medical devices (such as pacemakers, hearing aids, etc...) to determine if they are adequately shielded from external RF energy.

Turn your terminal **OFF** in health care facilities when any regulations posted in the area instruct you to do so. Hospitals or health care facilities may be using RF monitoring equipment.

6.2.2.5 Aircraft

Turn your terminal OFF before boarding any aircraft.

- Use it on the ground only with crew permission.
- Do not use it in the air.

To prevent possible interference with aircraft systems, Federal Aviation Administration (FAA) regulations require you to have permission from a crew member

to use your terminal while the aircraft is on the ground. To prevent interference with cellular systems, local RF regulations prohibit using your modem while airborne.

6.2.2.6 Children

Do not allow children to play with your GSM terminal. It is not a toy. Children could hurt themselves or others (by poking themselves or others in the eye with the antenna, for example). Children could damage the modem, or make calls that increase your modem bills.

6.2.2.7 Blasting areas

To avoid interfering with blasting operations, turn your unit OFF when in a « blasting area » or in areas posted : « turn off two-way radio ». Construction crew often use remote control RF devices to set off explosives.

6.2.2.8 Potentially explosive atmospheres

Turn your terminal **OFF** when in any area with a potentially explosive atmosphere. It is rare, but your modem or its accessories could generate sparks. Sparks in such areas could cause an explosion or fire resulting in bodily injuries or even death.

Areas with a potentially explosive atmosphere are often, but not always, clearly marked. They include fuelling areas such as petrol stations ; below decks on boats ; fuel or chemical transfer or storage facilities ; and areas where the air contains chemicals or particles, such as grain, dust, or metal powders.

Do not transport or store flammable gas, liquid, or explosives, in the compartment of your vehicle which contains your terminal or accessories.

Before using your terminal in a vehicle powered by liquefied petroleum gas (such as propane or butane) ensure that the vehicle complies with the relevant fire and safety regulations of the country in which the vehicle is to be used.

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