WISMO-CDMA

Dual-Band Embedded Module Hardware Specification

Reference: **WM_HWD_Q2338_PTS_001**
Level: **4.0**
Date: **23 Sept 2002**

PRELIMINARY

Document Information

Level	Date	History of the evolution	Writer
Rev 1	12/17/01		CNowak
Rev 2	03/07/02		CNowak
Rev 3	09/23/02	Board V3 update	CNowak
Rev 4	09/24/02	Audio update, formatting, Mech Drwg, SB comments	RNixon

	Name	Function	Date	Signature
Written by	CNowak			
Checked by				
Approved by				

Distribution List

-

Contents

Figures

Tables

Overview

This document is intended to detail the Hardware Design of the Wavecom Q2338 CDMA Module, allowing the customer to understand the function, capabilities and interface of the Module.

1 WISMOCDMA Introduction

1.1 Scope

Code Division Multiple Access, a cellular technology also known as **IS-95,** competes with GSM technology for dominance in the cellular world. There are now different variations, but the original CDMA is now known as **cdmaOne.** Developed originally by Qualcomm and enhanced by Ericsson, CDMA is characterized by high capacity and small cell radius, employing spread-spectrum technology and a special coding scheme.
The Telecommunications Industry Association (TIA) adopted CDMA, in 1993. By December 2000, there were 80 million subscribers on **cdmaOne** systems worldwide. Over 35 countries have either commercial or trial activity ongoing.
Enhancing today's data capabilities is the 1XRTT CDMA standard - this next evolutionary step for **cdmaOne** operators will provide packet data rates up to 144 kbps, significant capacity increases as well as extended battery life for handsets. This development is based on 1XRTT technology into an embedded module.

1.2 Applicable Standards

- 14.4 kbps Data Services IS-707
- 14.4 kbps Radio Link Protocol and Inter-band Operations TSB-74
- Addendum 1 (to the IS-2000 standard) TIA/EIA/IS-2000 PN-4756 (Ballot Version)
- CDMA Data Services Revision for IS-95B IS-707A
- CDMA Data Services Revision for cdma2000 Rel. 0 IS-707A-1
- CDMA Dual-Mode Air Interface Standard IS-95A, IS-95B
- CDMA Voice Coder Standards IS-96
- cdma2000: Signaling Layer 2 Standard for Spread Spectrum Systems
- PN-4430 (Ballot Resolution Version 0.14, to be published as TIA/EIA-IS-2000.4)
- IS-95 adapted for 1900 MHz frequency band J-STD-008
- Medium Access Control (MAC) for cdma2000 Spread
- PN-4429 (Ballot Resolution Version, to be published as TIA/EIA-IS-2000.3)
- TIA/EIA-95-B
- Option 3: Enhanced Variable Rate (max 8 kbps) Voice Coder (EVRC) IS-127
- OTA Update: Roaming System Selection and Programming Block IS-683A
- Physical Layer Standard for cdma2000 Spread Spectrum Systems PN-4428 (Ballot Resolution Version, to be published as TIA/EIA-IS-2000.2)
- Short Message Service including mobile origination IS-637A
- Upper Layer (Layer3) Signaling Standard for cdma2000 Spread Spectrum Systems PN-4431 (Ballot Resolution Version 1.06, to be published as TIA/EIA-IS-2000.5)

1.3 Safety and Governmental Agency Approval

The WISMOCDMA CDMA module shall comply with the following standards or guidelines:

- Formal Qualification Test, as mutually specified by Wavecom and manufacturer.
- IEC950, for electrical safety
- UL950, for electrical safety
- FCC Part 15B power supply, conducted requirements only
- FCC Part 22 (800 MHz), Part 24 (1900 MHz)
- SAR

- CSA for Canada
- Canada IC-133
- CDG 1, 2, 3
- IS-98D

2 Product Features

2.1 General Specifications WISMOCDMA module:

– Support voice communication	Interface connector.
– Wireless interface	CDMA2000 (IS-95C)
– Wireless data rate	144 kbps
– Supporting OS	All via AT Commands
– Current consumption	
Receive Mode	Max 150mA
Transmission Mode	Max 770mA
Sleep Mode	3.8mA
– Dimension	58 x 32 x 5.9 mm (Including shielding)
– Weight	20 grams
– Operating Temperature	-30°C ~ +60°C
– Mode	CDMA
– Band (CDMA2000) – (Dual Band)	
Band class 0	(800MHz)
Band class 1	(USPCS 1900MHz)
– Test	RF Connector

2.2 RF Features

- WISMOCDMA CDMA module shall support Rx and Tx specifications per IS-98D and IS-95A/IS-95B, Sections 2.1.2 through 2.1.3.1.1, 2.1.4, 2.2.3, and 2.1.3.1.9 through 2.1.3.1.10 as well as the corresponding portions of Section 6.

- WISMOCDMA CDMA module shall pass CDG-2 and CDG-3 interoperability testing specifications on Lucent, Nortel and Motorola infrastructures.

2.3 Baseband Features

The WISMOCDMA uses the Qualcomm MSM5105 for its Baseband hardware.
The features of this solution include:

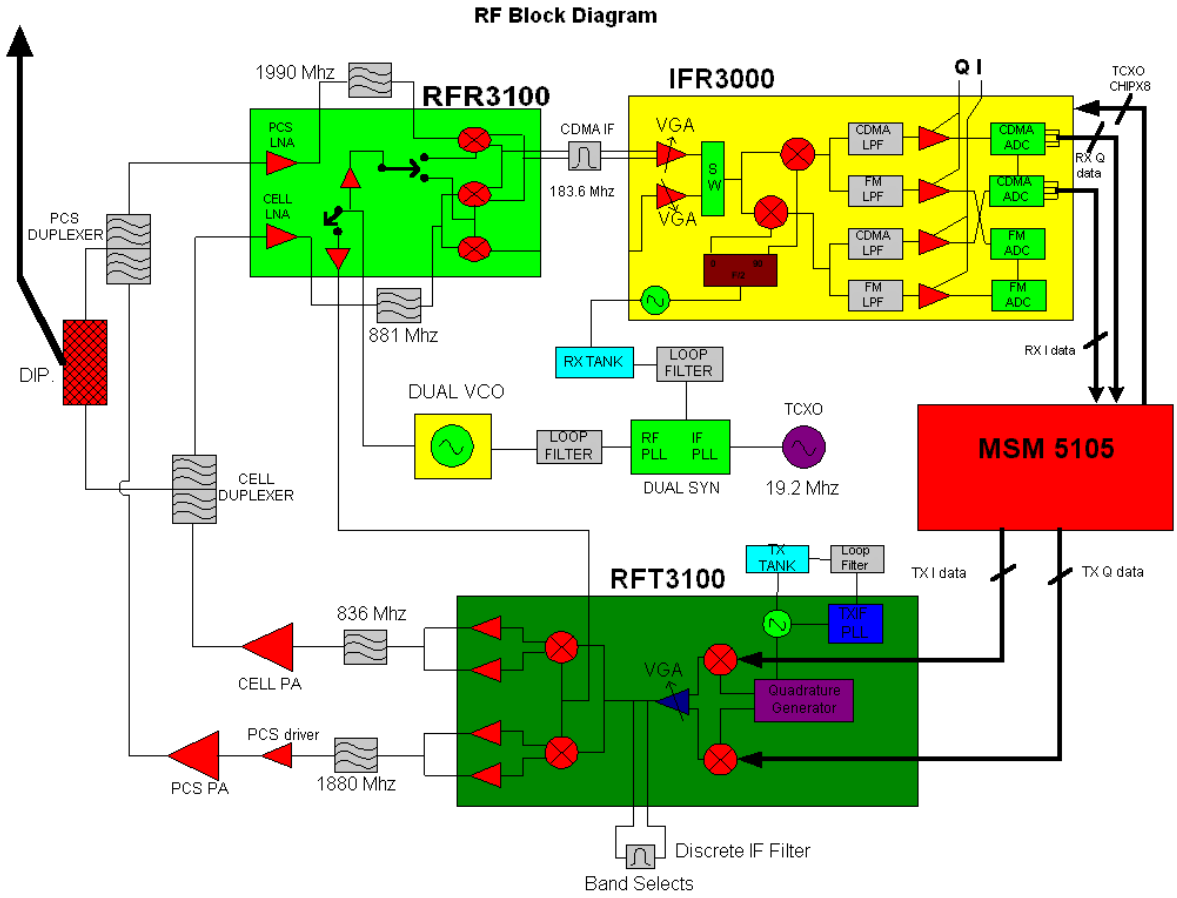
MSM5105
- Embedded QDSP2000 digital signal processor core, enabling features such as voice recognition, voice memo, speech compression, acoustic echo cancellation,
- 16-bit wide Flash and SRAM support
- Standard MIDI ringer
- Voice mode V1 (EVRC, IS-96A, PureVoice[a]), all radio configurations
- High-speed data using both fundamental and supplemental channels
- ARM7TDMI
- General-Purpose Interface Bus
- Microprocessor power down modes
- Internal watchdog and sleep timers

- Battery Management
- Charge Control
- Linear voltage regulation
- Programmable voltages for Digital and RF
- LCD Light driver
- Keypad Light driver
- Ringer driver
- Vibra driver
- RTC circuit
- SBI control

3 Detailed Description

3.1 RF

Figure 3-1 RF Block Diagram



NOTE: This drawing requires update to correctly reference the V3 Module design. Please use as general reference only.

3.1.1 Transmitter

3.1.1.1 RFT3100-1

- Full up conversion from analog base band to RF
- Integrated I/Q modulator, IF VCO/PLL, SSB up converter, VGA and driver amplifiers
- Eliminates image-reject filter between up converter and driver amplifier
- Includes two cellular and two PCS driver amplifier outputs
- MSM-controlled operation via Serial Bus Interface (SBI)
- TX power control through 85dB dynamic range VGA
- Puncture mode (gated TX power) for extended talk-time performance
- Supply voltage from 2.7 V to 3.3 V
- BCC++ 32-pad plastic chip scale package (5 mm x 5 mm x 0.8 mm)

3.1.1.2 Transmitter Specification

Transmitter performance test specification is CDMA2000 mobile station minimum requirement standard, **3GPP2 TSG C0011-A**.

- Operating Frequency	824MHz ~ 849MHz (Cellular Band) 1850MHz ~ 1910MHz (PCS Band)
- VCO Frequency Range	
- IF Frequency	
- Modulation	OQPSK
- Conversion Method	Heterodyne
- Oscillation Method	VCTCXO & PLL Synthesizer
- RF Output Power	
Maximum	0.2W
Minimum	10nW (-50dBm)
- Frequency Stability	+/- 300Hz
- Open Loop Power Control output Power	
RX= -25dBm	TX = -57.5 ~ -38.5dBm
RX= -65dBm	TX = -17.5 ~ +1.5dBm
RX= -104dBm	TX = +18 ~ +30dBm
- Spurious Emission	
RX band	-81dBm at 1MHz RBW
TX band	-61dBm at 1MHz RBW
Other Frequency	-47dBm at 30KHz RBW

3.1.2 Receiver

3.1.2.1 RFR3100

- Performs down conversion from RF to CDMA and FM IF
- Dual-band PCS/Cellular
- NF and IIP3 requirements for IS-98
- LNA Gain Control provided for improved dynamic range and Rx performance in the presence of high-level interferers.
- Selective power-down modes for extended standby-time performance
- Supply voltage from 2.7 V to 3.15 V
- 32-pin BCC++ plastic package (5 mm x 5 mm x 0.8 mm)

3.1.2.2 IFR3000

- The circuit blocks within the IFR3000 include the Rx AGC amplifier with 90 dB dynamic range, IF mixer and CDMA/FM low-pass filters for down-converting IF to

analog baseband, and analog-to-digital converters (ADC) for converting to digital base band.
- The IFR3000 includes clock generators that drive the digital processor and a voltage controlled
- Oscillator (VCO), which generates the Rx mixer local oscillator (LO) signal.
- 2.7 V to 3.15 V supply voltage
- Low current: 21 mA
- Rx power control through 90 dB dynamic range AGC amplifier
- IF mixer for down-converting IF to analog base band
- Low-pass filtering for CDMA
- 4-bit ADCs convert CDMA I and Q analog base band components to digital base band
- 8-bit ADCs convert FM I and Q analog base band to digital base band
- Clock generators for CDMA operation
- VCO for generation of Rx LO mixing signal and Q-channel DC offset control inputs drive baseband
- DC voltage offset to zero in CDMA signal path
- Selective power-down
- 48-lead BCC

3.1.2.3 Receiver Specification

Receiver performance test specification is CDMA2000 mobile station minimum requirement standard **3GPP2 TSG C.S0011-A**.

- Operating Frequency	869MHz ~ 894MHz (Cellular Band) 1930MHz ~ 1990MHz (PCS Band)
- VCO Frequency Range	
- IF Frequency	
- Modulation	QPSK
- Conversion Method	Heterodyne
- Oscillation Method	VCTCXO & PLL Synthesizer
- Receiver Sensitivity	-104dBm @FER 0.5%
- Single Tone Desensitization	-101dBm @ FER 1%
- (FC+/-900KHz @–30dBm)	
- IMD	-101dBm @ FER 1%
- (FC+/-900KHz, FC+/-1700KHz @–43dBm)	
	-90dBm @ FER 1%
- (FC+/-900KHz, FC+/-1700KHz @–36dBm)	
	-79dBm @ FER 1%
- (FC+/-900KHz, FC+/-1700KHz @–21dBm)	
- Conducted Spurious Emission	
RX band	-81dBm @1MHz RBW
TX band	-61dBm @1MHz RBW
Other Frequencies	-47dBm @30KHz RBW

3.1.3 Synthesizer

3.2 Baseband

The Baseband is composed of three basic blocks. The Blocks are Power, Digital Processing, and System Connector.

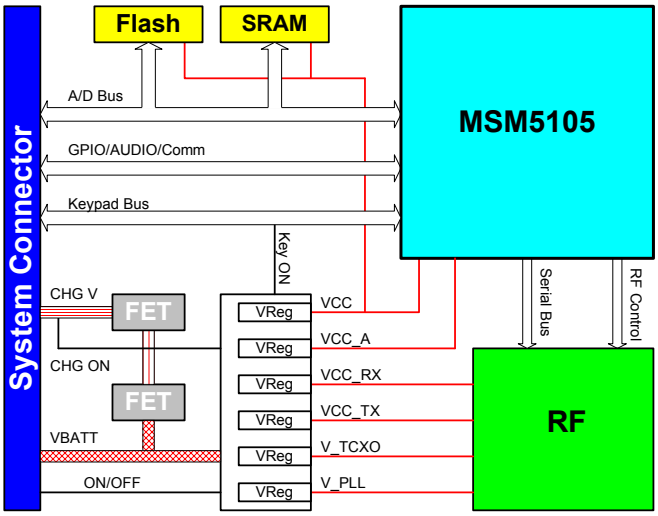
The Power block consists of six discrete regulators, which provide power to the module. A charging circuit is provided. If no battery charging is required then those parts may be left off without affecting the performance of the Power Block.

The Digital Processing block consists of the MSM5105 and two memory parts. The memory parts are industry standard SRAM and Flash components. The MSM5105 and the memory will be covered separately below.

The System Connector is a 60-pin dual row surface mount component. The overall board-to-board height is 3.0 mm. There are several zero ohm resisters on the opposite side of the connector that allow for various configurations of signals on the connector.

Each block will be covered in more detail below.

Figure 3-2 Baseband Block Diagram



3.2.1 Power

3.2.1.1 ON-OFF

There are three Modes for powering the module ON and OFF.

3.2.1.1.1 Mode One

A high input on pin 6 of the system connector cause the module to power ON. A low on pin 6 will cause the module to power OFF.

3.2.1.1.2 Mode Two

This Mode is a keypad input on pin 21 of the system connector. Pin 21 is Row_4 of the keypad system.

A low on this pin will cause the module to power ON, a subsequent low will cause the module to power OFF.

3.2.1.1.3 Mode Three

Mode Three is part of the charging circuit. When a voltage is applied to the charge pins then the module will power ON. The module will power OFF when charge voltage is removed if Software has not sensed a power ON from one of the other Modes.

3.2.1.2 Vcc_Out

Power out is provided on pin 40 of the System Connector. Vcc_Out goes active 20ms max after Power-On is sensed. The Vcc_Out is the same as system digital power and it will go low when the module is turned OFF. The module can provide up to 50mA to the outside system without affecting the module operation.

3.2.1.3 Charging

Charging is provided for Lithium Ion batteries only. The charging is a function of Software monitoring the voltage on the battery. The external charging input source should be a constant current and constant voltage type supply. The battery size is relative to the charger input.

3.2.2 Digital

3.2.2.1 MSM5101

3.2.2.2 Memory

The WISMOCDMA Module has both SRAM and Flash. The system memory bus has a 16-bit wide data bus and a 21-bit address bus. Control lines provide for single byte writes and reads of the SRAM.

WISMOCDMA memory is 512K bytes of SRAM and 2M bytes of Flash. The Flash is a read-while-write part containing both the executable code and non-volatile parameters such as Calibration data. The Flash size also allows for user applications needed in product design.

The Flash on the WISMOCDMA can be reprogrammed using the Wavecom Flash Download Window running on a PC.

3.2.3 System Connector

3.2.3.1 System Connector Description

The System Connector has 60 pins and provides the interface between the WISMOCDMA module and the OEM designer's platform. The connector has a 0.5 mm pitch and a stacking height of 3.0 mm. The connector manufacturer is Kyocera/AVX. The mating connector part number is 24-5087-060-X00-861.

3.2.3.2 I/O Description Parameters

Table 3-1 I/O Pin Parameters

Symbol	Description
Type	
B	Bi-directional
BS	Bi-directional with Schmitt trigger
CCS	Controlled Current Sink
CHV	Input Charging Voltage
I	CMOS input
IS	Input with Schmitt trigger
O	Output
V	Power
Special Circuitry	
A	Analog pad
PU	Contains internal pull-up device
PD	Contains internal pull-down device
KP	Contains an internal weak keeper device. Keepers cannot drive external busses
H	Digital input where input voltage level may reach up to 3.6 V
(1,2,5, etc.)	Values are the +/- maximum current drive strength in mA for output pins
n[m]	Variable drive strength pins. The number 'n' is the drive strength when the PAD_CTL register bit is clear (0). The Number [m] is the drive strength when the PAD_CTL bit is set (1).

3.2.3.3 System Connector Names and Pin Outs

Table 3-2 System Connector Pin Assignment

Pin #	Signal Name	Pin Type	Alt Function 1	Alt Function 2	R-#
1	CHG_IN				
2	CHG_IN				
3	R-UIM_CLK	O-3			
4	CHG_IN				
5	GPIO_INT_5	BS-PU1	R-UIM_RST		
6	ON_/OFF	BS-PU1			
7	R-UIM_Data	BS-PU3			
8	GPIO_INT_21	BS-PU3	TX2		
9-A	GPIO_INT_30	BS-PD5	R-UIM_PWR_EN		R903
9-B	/RD	BS-2[3]			R904
10	GPIO_INT_20	BS-PD1	RX2		
11	No Connect				
12	GPI_INT_42	BS-H2-KP		USB-DATA	
13	ROW_0	IS-PU	INT-0		
14	/RST_IO				
15	ROW_1	IS-PU	INT-1		
16	GPI_INT_44	BS-H2-KP		USB-VPI	
17	ROW_2	IS-PU	INT-2		
18	GPI_INT_43	BS-H2-KP		USB-VMI	
19	ROW_3	IS-PU	INT-3		
20-A	GPIO_INT_13	BS-PD3			R929
20-B	Data-0	B-KP2[3]			R931
21	ROW_4	IS-PU	INT-4		
22-A	GPIO_INT_14	BS-PD3-KP			R932
22-B	Data-1	B-KP2[3]			R933
23	GPIO_INT_47	BS-KP3	COL_0	USB-VPO	
24-A	GPIO_INT_16	BS-PD3-KP		USB-SUSPND	R934
24-B	Data-2	B-KP2[3]			R936
25	GPIO_INT_46	BS-KP3	COL_1	USB-VMO	
26-A	GPIO_INT_10	BS-PU3-KP			R937

26-B	Data-3	B-KP2[3]			R938
27	GPIO_INT_45	BS-PU3	COL_2	USB-OE	
28-A	GPIO_INT_36	BS-PU3-KP			R939
28-B	Data-4	B-KP2[3]			R940
29	GPIO_INT_23	BS-PU3-KP	COL_3		
30	RS232-RTS	IS-PD			
31	GPIO_INT_22	BS-PU3-KP	COL_4		
32	RS232-RX	O-3			
33	ADC_0	IA			
34	GPIO_INT_2	BS-PU2[3]	DTR		
35-A	GPIO_INT_7	BS-PU1			R923
35-B	Data-5	B-KP2[3]			R924
36-A	GPIO_INT_3	BS-PU2[3]	DSR		R942
36-B	A1	B-2[3]			R943
37	RS232-CTS	O-3			
38	ADC_1	IA			
39	RS232-TX	IS-PD			
40	VCC-Out_2.8v				
41	SPK_2P	OA			
42	MIC_2P	IA			
43	AGND				
44	MIC_2N	IA			
45	SPK_1P	OA			
46	MIC_1P	IA			
47	SPK_1N	OA			
48	MIC_1N	IA			
49	BUZ	O-5			
50	GPIO_INT_40	BS-PU2[3]		LCD_CS	
51-A	GPIO_INT_4	BS-PU3			R918
51-B	Data-6	B-KP2[3]			R919
52	GPIO_INT_9	BS-PD3-KP			
53-A	GPIO_INT_8	BS-PD1			R927
53-B	/WR	BS-PU2[3]			R928
54-A	GPIO_INT_11	BS-PU3-KP			R921
54-B	Data-7	B-KP2[3]			R922

55	+Vbatt				
56	VIBRA	O-1			R946
57	+Vbatt				
58	+Vbatt				
59	+Vbatt				
60	+Vbatt				

3.2.3.4 GPx_INT

There are 25 General Purpose IO Interrupt pins on the System Connector. Three of the pins are Input Interrupt pins only. Depending on product requirements, 17 GPIO pins can be configured for various functions. There are 7 GPIO_INT pins that are jumper configurable with other signals, these are shown in Table 3.2 as Pin #-A or B. All GPIO pins can be configured as interrupts to the system. Table 3-3 shows the alternate functions for each pin. Some pin configurations can only be done in blocks or multiple sets of pins.

Table 3-3 Signal Name and Alternate Function

Pin #	*Signal Name*	*Pin Type*	*Alt Function 1*	*Alt Function 2*
5	GPIO_INT_5	BS-PU1	R-UIM_RST	
8	GPIO_INT_21	BS-PU3	TX2	
9-A	GPIO_INT_30	BS-PD5	R-UIM_PWR_EN	
10	GPIO_INT_20	BS-PD1	RX2	
12	GPI_INT_42	BS-H2-KP		USB-DATA
16	GPI_INT_44	BS-H2-KP		USB-VPI
18	GPI_INT_43	BS-H2-KP		USB-VMI
20-A	GPIO_INT_13	BS-PD3		
22-A	GPIO_INT_14	BS-PD3-KP		
23	GPIO_INT_47	BS-KP3	COL_0	USB-VPO
24-A	GPIO_INT_16	BS-PD3-KP		
25	GPIO_INT_46	BS-KP3	COL_1	USB-VMO
26-A	GPIO_INT_10	BS-PU3-KP		
27	GPIO_INT_45	BS-PU3	COL_2	USB-OE
28	GPIO_INT_36	BS-PU3-KP		
29	GPIO_INT_23	BS-PU3-KP	COL_3	
31	GPIO_INT_22	BS-PU3-KP	COL_4	
34	GPIO_INT_2	BS-PU2[3]	DTR (I)	

35-A	GPIO_INT_7	BS-PU1		
36-A	GPIO_INT_3	BS-PU2[3]	DSR (O)	
50	GPIO_INT_40	BS-PU2[3]		
51	GPIO_INT_4	BS-PU1	DCD (O)	
52	GPIO_INT_9	BS-PD3-KP		USB-SUSPND
53	GPIO_INT_8	BS-PD1		
54	GPIO_INT_11	BS-PU3-KP	RI (O)	

3.2.3.5 Keypad

The WISMOCDMA module provides for a 5 x 5 keypad matrix. The five Rows are used to sense key contact closure when connected to an external keypad. The Row pins have active pull-ups built in to reduce the need for external components. ROW pins are dedicated inputs that are mapped to the Interrupt Controller. If the Row pins are used in a keypad they can still be used as interrupt inputs. See Figure 3-3 for Interrupt sense circuit. The five Columns are multi-function GPIO_INT pins. When the GPIO_INT pins are used as Columns their other functions are unavailable. Figure 3-4 shows the Row and Column pins on the System connector.

Figure 3-3 Interrupt Sense Circuit

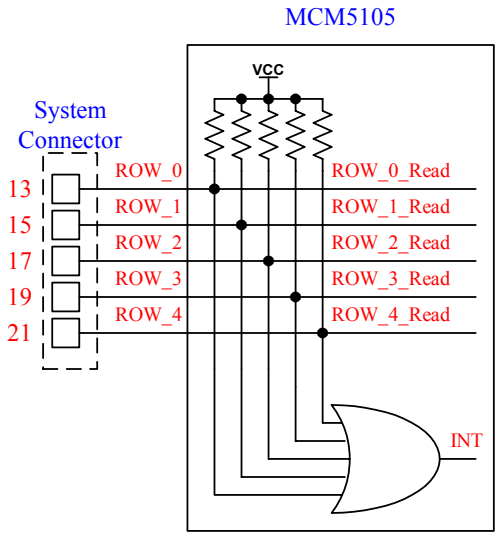
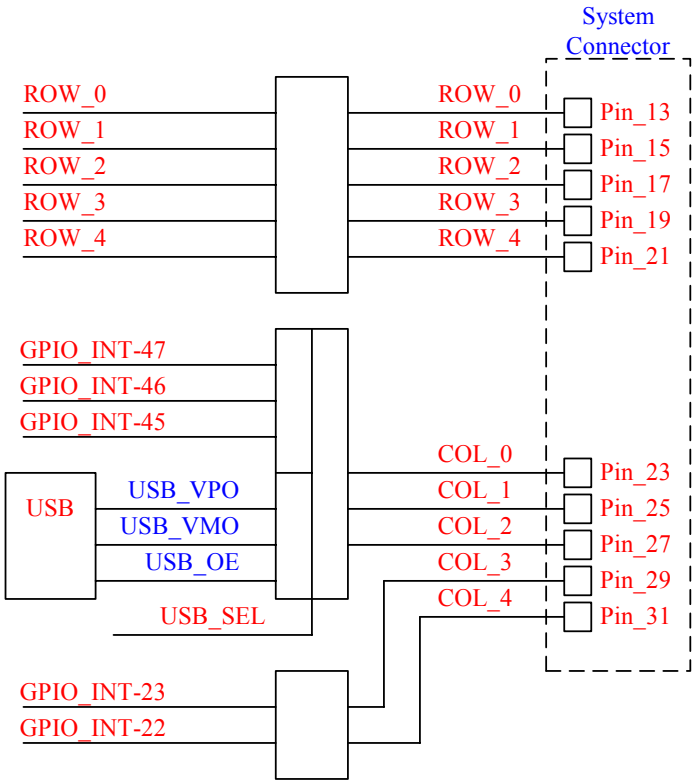


Figure 3-4 Multiplexing Arrangement for Keypad Columns



3.2.3.6 I/O Interfaces

The WISMOCDMA module has 5 external communication Interfaces. Each Interface and its functions are described below. Not all the Interfaces can be used at the same time.

3.2.3.6.1 UART – 1

The UART communicates with serial data that conforms to RS-232 interface protocol. The UART is fully configurable by SW. UART_1 has 4 dedicated pins on the System Connector these are shown in Table 3-4

Table 3-4 UART-1 Pin Names and Numbers

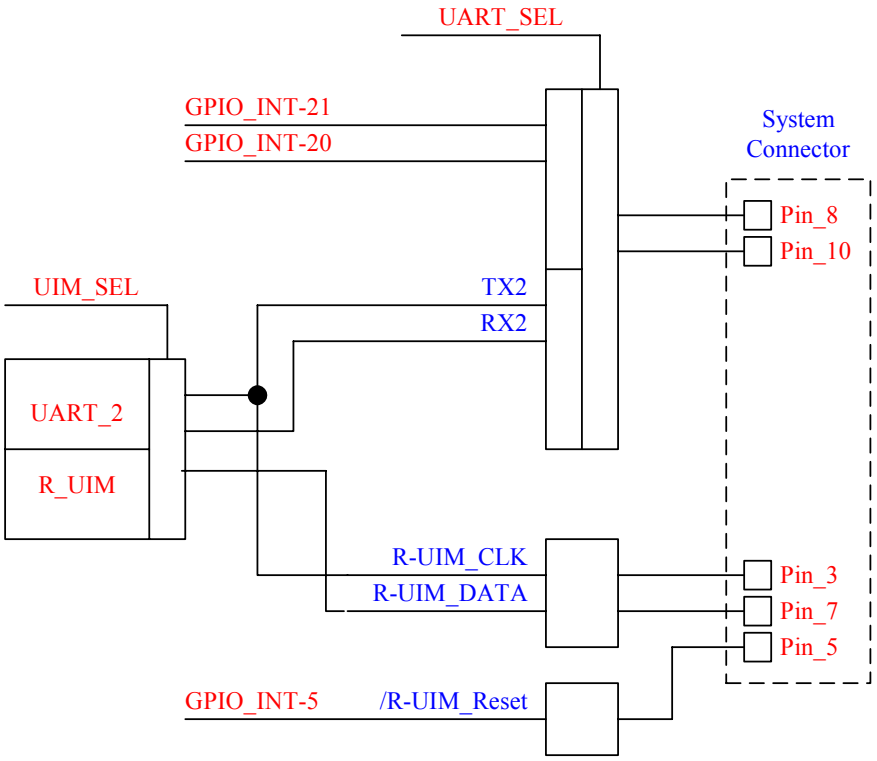
Signal Name	Description	Sys. Conn. #
RS232_RX	Transmit serial data (OUTPUT)	32
RS232_TX	Receive serial data (INPUT)	39
RS232_RTS	Clear to send (INPUT)	30
RS232_CTS	Request to send (OUTPUT)	37

3.2.3.6.2 UART – 2

The UART communicates with serial data that conforms to RS-232 interface protocol. The UART is fully configurable by SW.

UART-2 uses pins 8 and 10 on the System Connector. When UART-2 is selected, R_UIM and GPIO_INT 20 and 21 are not available. When the UART is not selected all GPIO_INT signals and R_UIM signals can be used. Figure 3-5 shows the multiplexing scheme for UART-2.

Figure 3-5 Multiplexing Arrangement for UART-2



3.2.3.6.3 R-UIM

The R-UIM Interface provides for communication with a CDMA smart card. The R-UIM controller shares functions with the UART, as seen in Figure 3-tt. When the R-UIM is enabled the UART is disabled, but the GPIO_INT signals available for use.

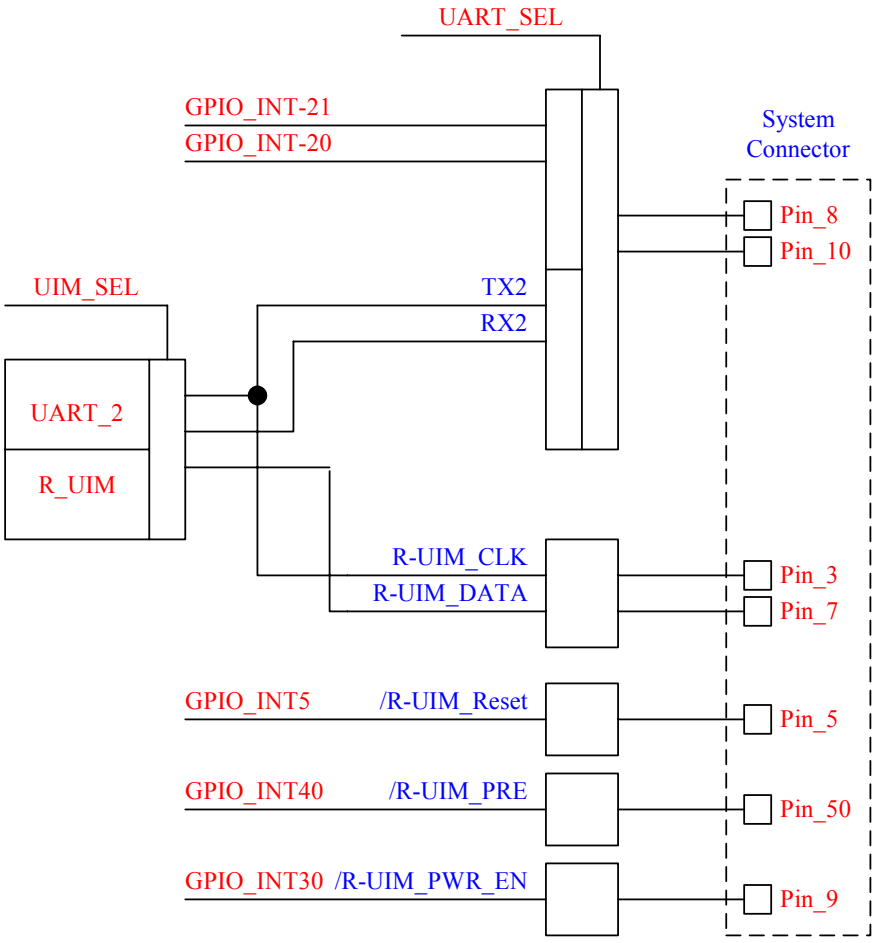
The R-UIM Interface consists of Clock, Data, Pwr_En, Pre, and Reset signals. The Clock and Data are part of the UART block, but the Pwr_En, Pre, and Reset (Control) signals are GPIO_INT lines. The Control signals are under SW control. When the R-UIM is not in use

the Control lines are available for User defined functions. Figure 3-6 shows the multiplexing scheme for R-UIM.

R-UIM power is controlled by the Pwr_En signal. This signal is used to enable an LDO regulator in order to supply power to the R-UIM. The R-UIM has a maximum constant current draw of 50 mA and can spike to 50 mA above this level. Refer to the R-UIM specification for further details.

The R-UIM Present signal is not defined in the R-UIM space. This signal maybe a function of the R-UIM card holder. This signal need not be used, as the SW will be configured for an R-UIM if one is capable of being used.

Figure 3-6 Multiplexing Arrangement for R-UIM

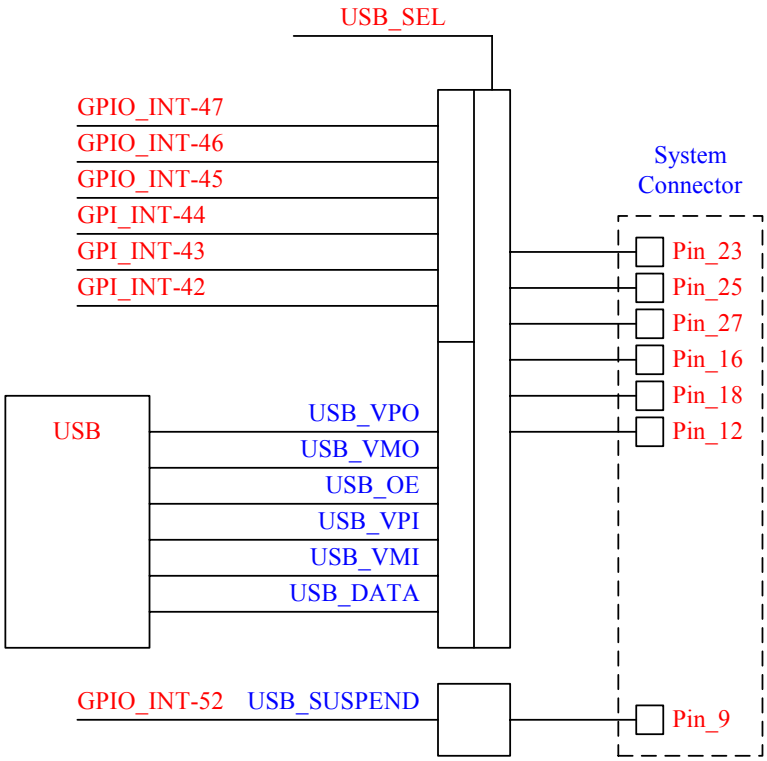


3.2.3.6.4 USB

The WISMOCDMA System Connector contains a USB interface to provide an efficient interconnection between modem and OEM products. The WISMOCDMA USB interface is USB Rev 1.1 compliant. An external USB transceiver is required to implement the interface.

The USB signals are multiplexed with GPIO_INT [0,1,2,6] and GPI_INT [3,4,5], as selected by SW. When the USB is configured the GPx_INT signals are not available. Figure 3-7 shows the multiplexing scheme for the USB.

Figure 3-7 Multiplexing Arrangement for USB



The USB interface supports connections to transceivers with both separate input and output data pins (Philips PDIUSBP11) or with bi-directional data pins (Micrel MIC2550). Selection of the transceiver type is done by SW.

The following figures show the connections between the System Connector and the two transceivers.

Refer to the appropriate data sheet for each transceiver connection requirements.

Figure 3-8 Example Connections for Philips PDIUSBP11 Transceiver

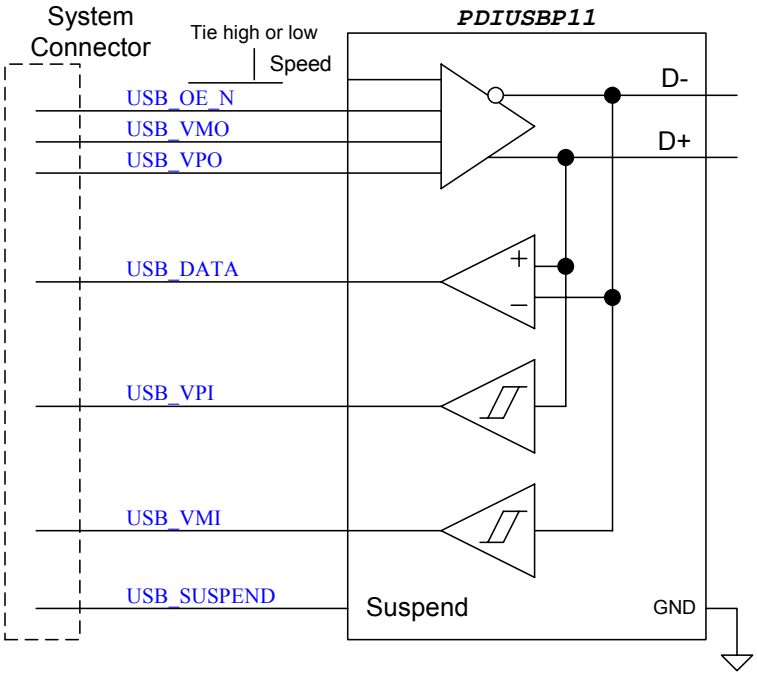
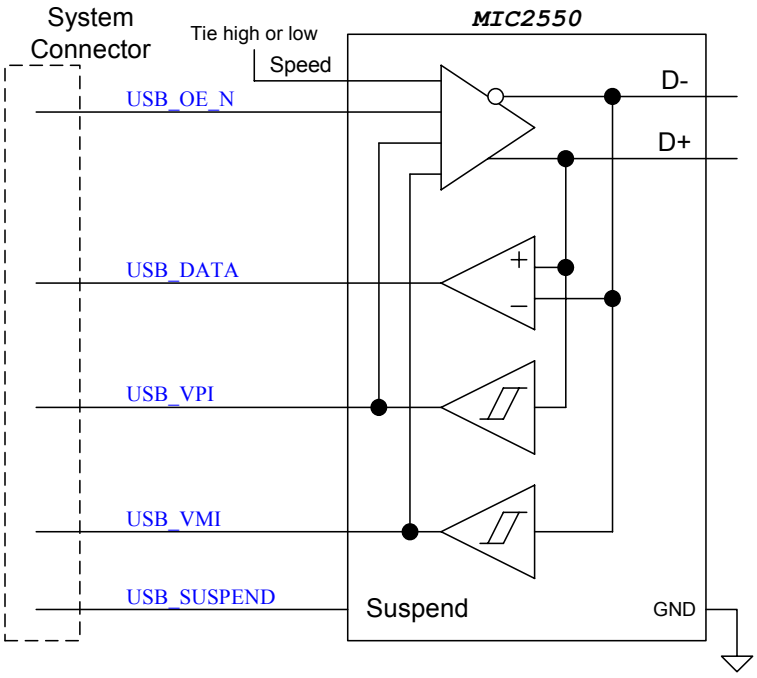


Figure 3-9 Example Connections for Micrel MIC2550 Transceiver



3.2.3.6.5 LCD

The WISMOCDMA module has a parallel interface for connecting to an LCD display. Pin 40 provides power to external circuits that will be powered down when the module is OFF. See Table 3-5 for a complete list of pin names and numbers. Read is available on pin 14 when jumper B is installed. The interface can be used for communication with any device that needs a parallel interface.

Table 3-5 LCD Pin Numbers and Names

Pin #	Signal Name	Function
40	Vcc_OUT	Supply Voltage to LCD
50	LCD_CS	Chip Select
51	LCD_D/C	Data or Command select
53	/WR	Write
9	/RD	Read
36	A1	Address 1
20	Data0	Data 0
22	Data1	Data 1
24	Data2	Data 2
26	Data3	Data 3
28	Data4	Data 4
35	Data5	Data 5
51	Data6	Data 6
54	Data7	Data 7

3.2.3.7 General Purpose ADC

The System Connector has 2 General Purpose Analog-to-Digital Converter (GPADC) inputs. Bat_Temp is found on pin 33 and ADC_0 is on pin 38. The 2 inputs are multiplexed into 1 10-bit ADC, Table 3-6 shows the ADC Analog Input Spec. Software controls which ADC is being read.

Table 3-6 GPADC Analog Input Spec.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Channel Isolation		f </= 1KHz	38	50		dB
Top Reference Voltage	VRT		2.425	2.5	2.575	V
Full Scale input voltage			6.5 mV		VRT	V

Input Bandwidth		With 200K source impedance			1.0	KHz
Input Resistance			3			M ohm
Input Capacitance					10	pF

3.2.3.8 Audio/Alert

The WISMOCDMA provides audio input and output on the System Connector. The System Connector provides for two MICs and two Speakers to be connected, with either pair being selectable via AT Commands.

3.2.3.8.1 MIC

The WISMOCDMA System Connector provides two microphone interfaces to the main board. Both the primary interface (MIC_1) and secondary (MIC_2) are differential interfaces. Either can of course be used in a single-ended application (such as for a headset) however the differential configuration is recommended to help reduce noise.

Figure 3-10 is example of a differential microphone in a typical handset application.

Figure 3-10 MIC_1 Differential Interface

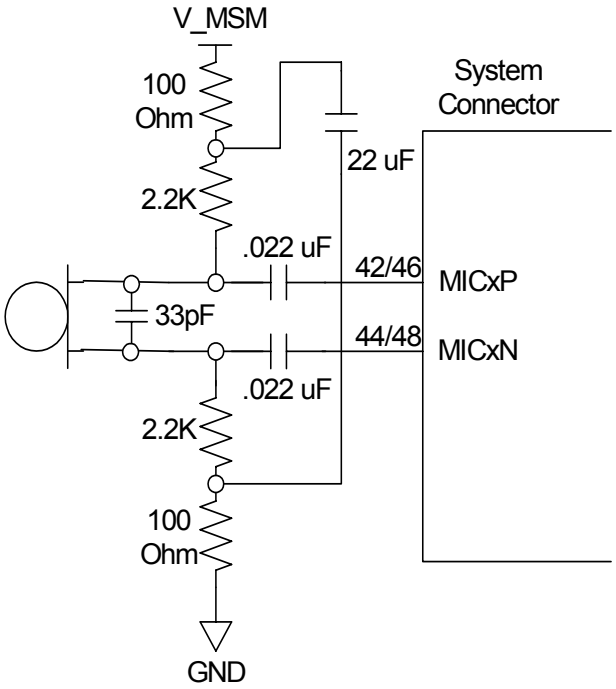
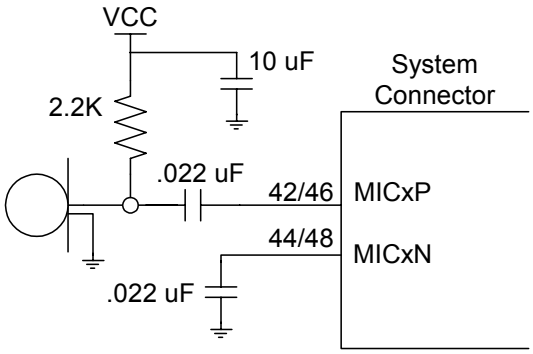


Figure 3-11 is example of a single-ended microphone in a typical handset application.

Figure 3-11 MIC_2 Single-Ended Interface



3.2.3.8.2 Speaker

The WISMOCDMA System Connector provides two speaker interfaces to the main board. The primary interface (SPK_1) is a differential interface. The secondary interface (SPK_2) is single-ended. The single-ended application is normally used for the headset. The output power for the differential SPK_1 is 35mW for a full-scale +3 dBm0 sine wave into a 32-OHM speaker. The output power for the single-ended SPK_2 is 8.8mW for a full-scale +3 dBm0 sine wave into a 32-OHM speaker.

Figure 3-12 is example of a differential speaker in a typical handset application.

Figure 3-12 SPK_1 Differential Interface

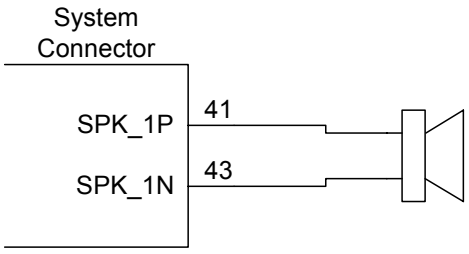
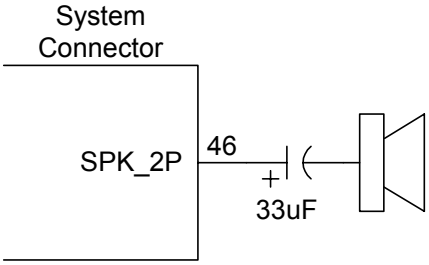


Figure 3-13 is example of a single-ended speaker in a typical handset application.

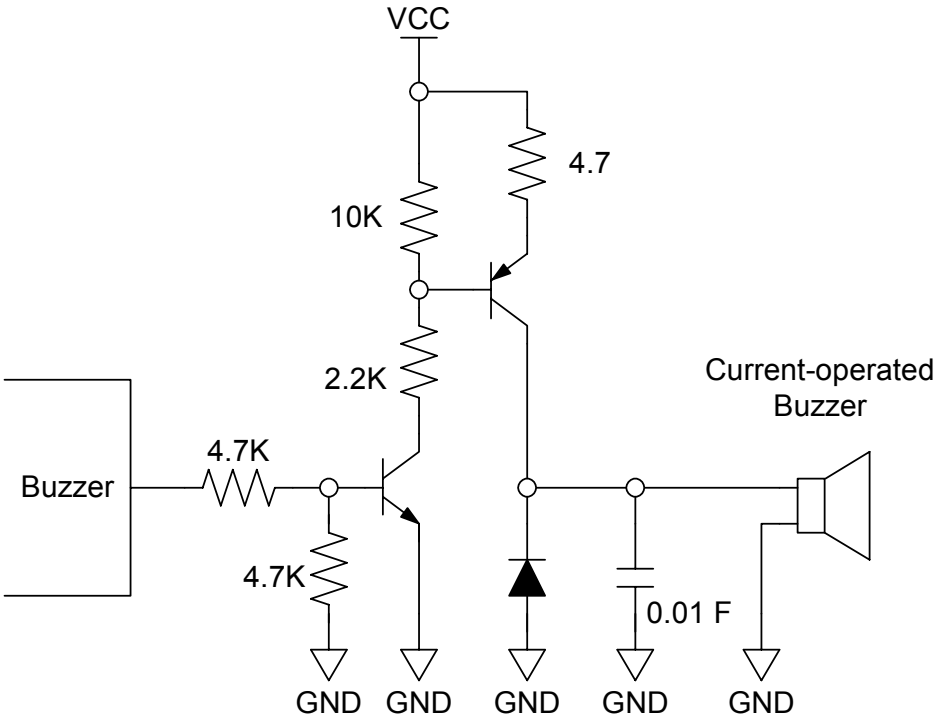
Figure 3-13 SPK_2 Single-Ended Interface



3.2.3.8.3 Ringer

SW controls the Ringer generation circuit. The signal on the Ringer pin of the System Connector is a digital pulse stream. The pulse stream can be a single tone or the sum of two different frequencies or DTMF tones.. Figure 3-14 shows a typical application.

Figure 3-14 Ringer Circuit



3.2.3.8.4 Vibra

The Vibra output is controlled by Software. The signal on the Vibra pin of the System Connector is a digital pulse stream. The circuit needed to run the Vibra motor is

dependant on the device being used. Refer to the manufacturers requirements for the appropriate drive circuit.

3.2.3.9 CDMA – GSM/GPRS Design Differences

Although the pin outs for both the CDMA Module with the GSM/GPRS Module designs are identical, and every attempt has been made to ensure the complete compatibility of the designs, there are some particular areas where care must taken to allow a “plug and play” swap of the two Module families.

3.2.3.9.1 Power Supply

The maximum voltage of the CDMA Module is 4.2Vdc. The GSM Module maximum is 4.5Vdc.

3.2.3.9.2 ON/OFF

The input voltage range on this line is 2.4-3.0Vdc for the CDMA Module. The GSM Module can accept an input of 2.4-5.0Vdc.

3.2.3.9.3 BOOT

To allow the customer to download new firmware into the Module, the GSM design requires the use of the BOOT line. The CDMA design does not require this line. This line on the CDMA Module is treated as a GPIO.

3.2.3.9.4 Audio

The CDMA Module provides only a single ended driver for the second speaker audio path. The GSM family has a differential driver here. Although any external circuit design making use of the differential drive will be compatible with the CDMA Module, the CDMA Module will have a relatively reduced drive level on this audio speaker path compared to the GSM.

3.2.3.9.5 Buzzer

The GSM Module provides a high level current sink on pin 49, allowing the direct connection of an external buzzer/ringer to the Module. The CDMA Module only provides a logic level control signal, requiring an external transistor circuit to properly drive the external buzzer/ringer.

4 Electrical Specification

4.1 DC Electrical Specifications

4.1.1 Absolute Maximum Ratings

Operating the WISMOCDMA under conditions that exceed those listed in Table 4-1 may result in damage to the device. Absolute maximum ratings are limiting values, and are considered individually, while all other parameters are within their specified operating ranges. Functional operation of the WISMOCDMA under any other conditions in Table 4-1 is not implied.

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage temperature	TS	-55	+150	C
Supply voltage (Battery)	VBATT	-0.5	4.2	Vdc
Supply voltage (Charger)	CHG_IN	-0.5	4.2	Vdc
Voltage applied to any input or output pin	Vin	-0.5	VCC + 0.5	Vdc

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Ambiant operating temperature	TS	-30	-	+60	C
Battery supply voltage	VBATT	3.6	-	4.2	Vdc
Charger supply voltage	CHG_IN	4.2	4.2	4.2	Vdc

4.1.3 DC Characteristics

Table 4-3 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
High-level input voltage, CMOS/Schmitt	V_IH	0.65xVccP	-	VccP+0.3	Volts
Low-level input voltage, CMOS/Schmitt	V_IL	-0.3	-	0.35xVccP	Volts
Input high leakage current	I_IH	-	-	2	uA
Input low leakage current	I_IL	-2	-	-	uA
Input high leakage current with pull-down	I_IHPD	10	-	60	uA
Input low leakage current with pull-up	I_ILPU	-60	-	-10	uA
High-level, three-state leakage current	I_OZH	-	-	2	uA
Low-level, three-state leakage current	I_OZL	-2	-	-	uA
High-level, three-state leakage current with pull-down	I_OZHPD	10	-	60	uA
Low-level, three-state leakage current with pull-up	I_OZLPU	-60	-	-10	uA
High-level, three-state leakage current with keeper	I_OZHKP	-25	-	-3	uA
Low-level, three-state leakage current with keeper	I_OZLKP	3	-	25	uA
High-level output voltage, CMOS	V_OH	VccP-0.45	-	VccP	Volts
Low-level output voltage, CMOS	V_OL	0.0	-	0.45	Volts
Input capacitance	C_IN	-	-	15	pF
ADC Full-Scale Input Range	A_FS	GND	-	V_RT	-
ADC Input Serial Resistance	A_ISR	-	5	-	Kohm
ADC Input capacitance	A_C_IN	-	12	-	pF
Input offset voltage at MIC1, MIC2	MV_IO	-5	-	+5	mV
Input bias current at MIC1, MIC2	MI_IB	-200	-	+200	nA
Input capacitance at MIC1, MIC2	M_CI	-	5	-	pF
Input DC Common Mode Voltage	-	0.85	0.9	0.95	V
Microphone Bias supply voltage	MBIAS	1.69	1.8	1.91	V
MBIAS Output DC source current	-	1	1.07	-	mA
Input impedance MIC1, MIC2	M_ZIN	62	72	82	Kohm

4.2 Power Consumption

Table 4-4 Power Consumption

Operating Mode	Band	Average	Units	Notes
		HI_Power = 3.0v		
CDMA RxTx Full Power	Cellular	615	mA	
	PCS	770		
CDMA RxTx Average Power	Cellular	340	mA	
	PCS	445		
CDMA Rx Active	Cellular	TBD	mA	
	PCS	TBD		
CDMA Sleep	Cellular	3.8	mA	
	PCS	3.8		

5 Mechanical

Figure 5-1 Module Mechanical Drawing